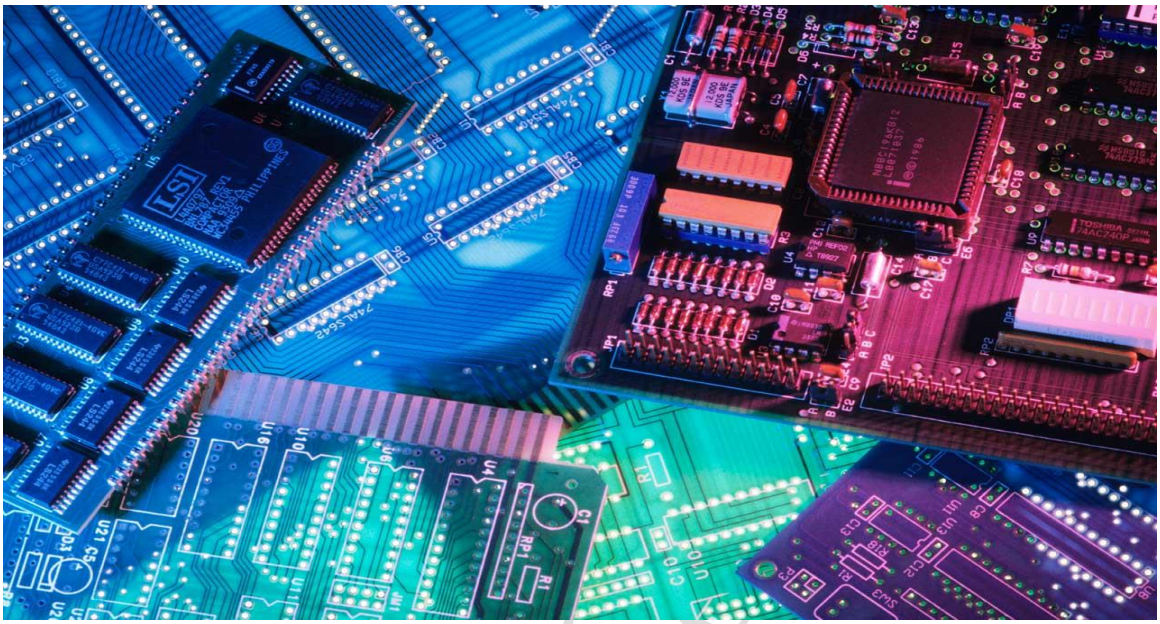
ELECTRONIC DEVICES and CIRCUITS

II B.TECH I SEMESTER-ECE



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

LENDI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institute, Approved by A.I.C.T.E & Permanently Affiliated to JNTU-GV, Vizianagaram)

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EDC Brief Notes Prepared by

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Electronic Devices and Circuits

S.NO	Unit Name	No. of Classes
1	P-N Junction Diode Characteristics & Special Diodes	9
2	Bipolar Junction Transistor (BJT) Characteristics	9
3	Field Effect Transistor (FET) Characteristics	10
4	Transistor biasing, Thermal Stabilization and h-Parameter Amplifier Analysis	10
5	Small Signal Transistor Amplifier Circuits	10

UNIT- I

Junction Diode Characteristics, Special Semiconductor Diodes

CLASS-1

Qualitative Theory of the P-N junction:

Open Circuited PN Junction (PN Junction diode in Equilibrium with no applied Voltage)

When a semiconductor is doped with P-type material on one side and N-type material on the other, a PN junction is formed. The N-type side has many free electrons, while the P-type side has many holes.

At the junction, electrons from the N-side move to the P-side, and holes from the P-side move to the N-side. This movement is called diffusion. As electrons leave the N-side, it becomes positively charged, and as electrons fill holes on the P-side, it becomes negatively charged.

This charge buildup creates a barrier that stops further movement of electrons and holes. The region near the junction, where no free carriers are left, is called the depletion region. The electric field formed across this layer creates a potential barrier (Vo) that prevents further charge movement. This voltage depends on the material and temperature, being about 0.3V for Germanium (Ge) and 0.72V for Silicon (Si).

When no external voltage is applied (V = 0V), the depletion region remains, and only fixed positive and negative ions are present, preventing further movement of electrons and holes.

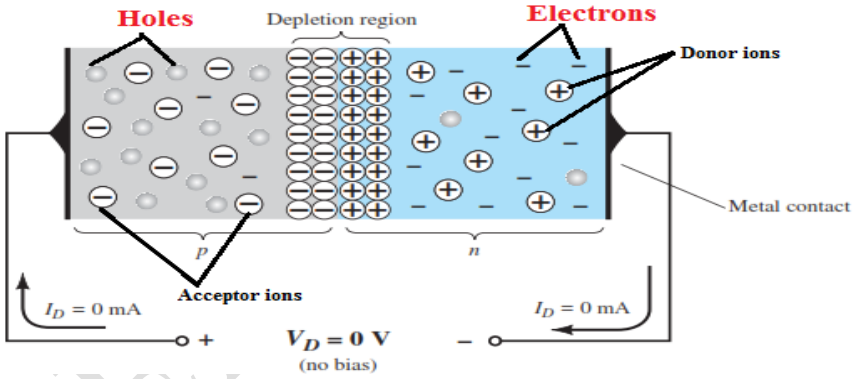


Figure : No bias Semi Conductor Diode

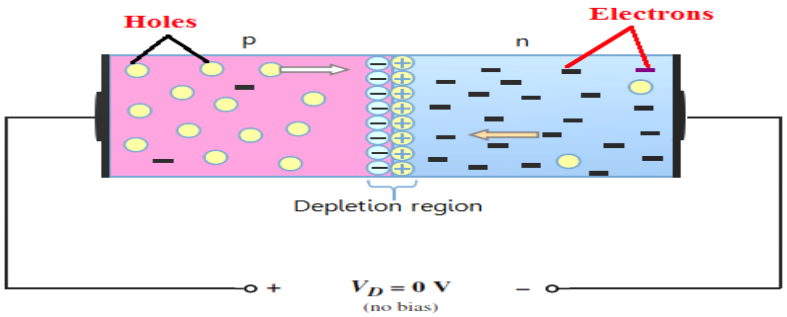
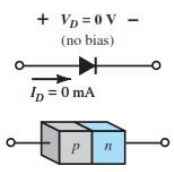


Figure : No bias Semi Conductor Diode without ions



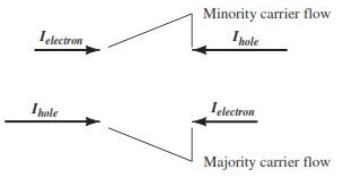


Figure :Symbol of PN Junction Diode

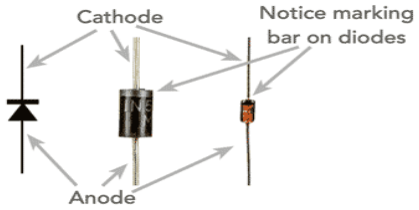


Figure : Physical Representation of PN Junction Diode

The electric field created by the positive charge in the N-type region pushes holes away from the junction, while the negative charge in the P-type region pushes electrons away.

As holes leave the P-region, they expose negatively charged acceptor atoms, creating a negative space charge in what was once a neutral area. Similarly, as electrons leave the N-region, they expose positively charged donor atoms, creating a double space charge at the junction.

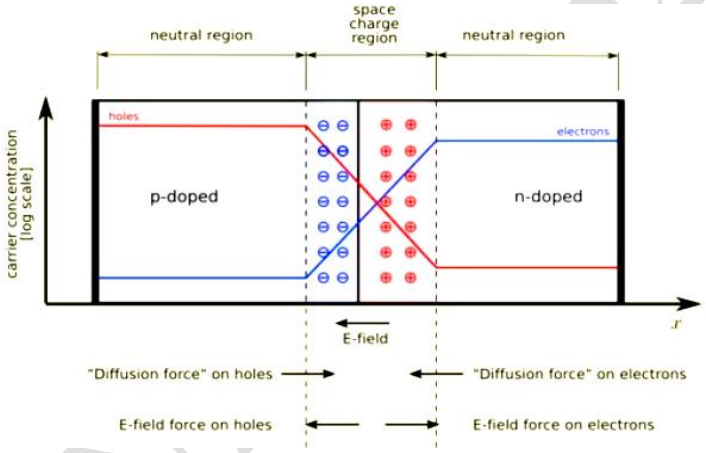


Figure : Diffusion of holes and electrons in P-N Diode

The space charge layers have opposite charges to the majority carriers trying to diffuse into them. This slows down diffusion.

This buildup of charge creates an electric field across the junction, from the N-region to the P-region, which prevents further movement of electrons and holes. The exact shape of the charge distribution depends on how the diode is doped.

Since there are no free-moving charge carriers in this region, it is called the depletion layer, space region, or transition region. It is about 0.5 µm thick.

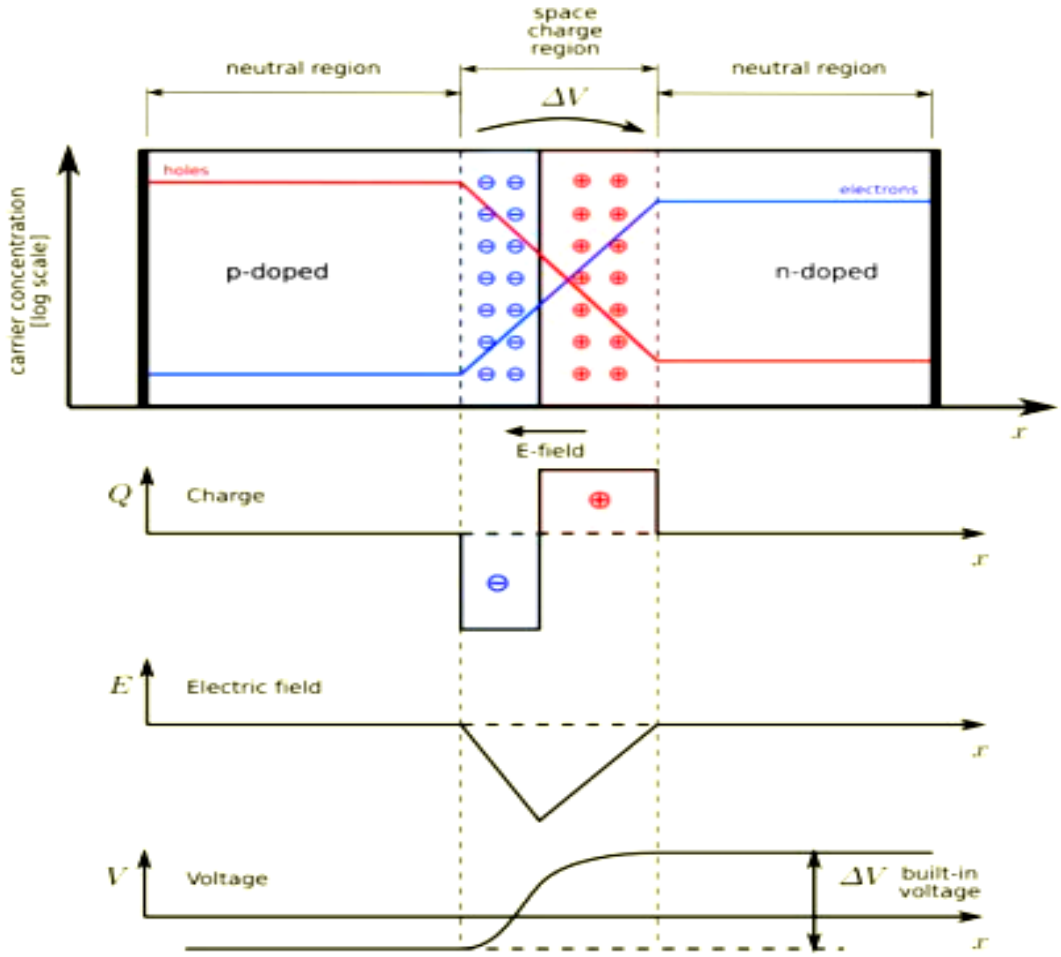


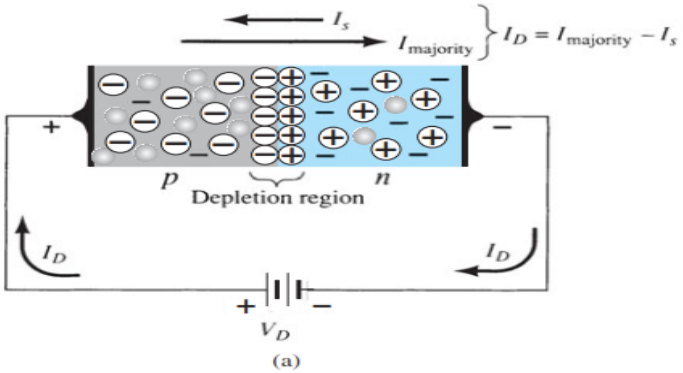
Figure : Diffusion of holes and electrons in P-N Diode

Biased P-N Junction

Forward-Bias Condition (V_D> 0 V):

A forward bias is created by connecting the positive terminal to the P-type material and the negative terminal to the N-type material.

This applied voltage (VD) pushes electrons in the N-region and holes in the P-region toward the junction. As they recombine with ions near the boundary, the depletion region narrows. This allows minority carriers to flow across the junction.



In a forward-biased PN junction, the flow of minority carriers (electrons from P to N and holes from N to P) stays the same because it depends on the fixed number of impurities in the material. As the applied voltage increases, the depletion region continues to shrink, allowing more electrons to pass through. This causes the current to rise exponentially, as shown in the forward-bias curve (Fig. 1.16).

The voltage across a forward-biased diode is usually less than 1V, and the current rises sharply after reaching a certain point on the curve, known as the knee voltage.

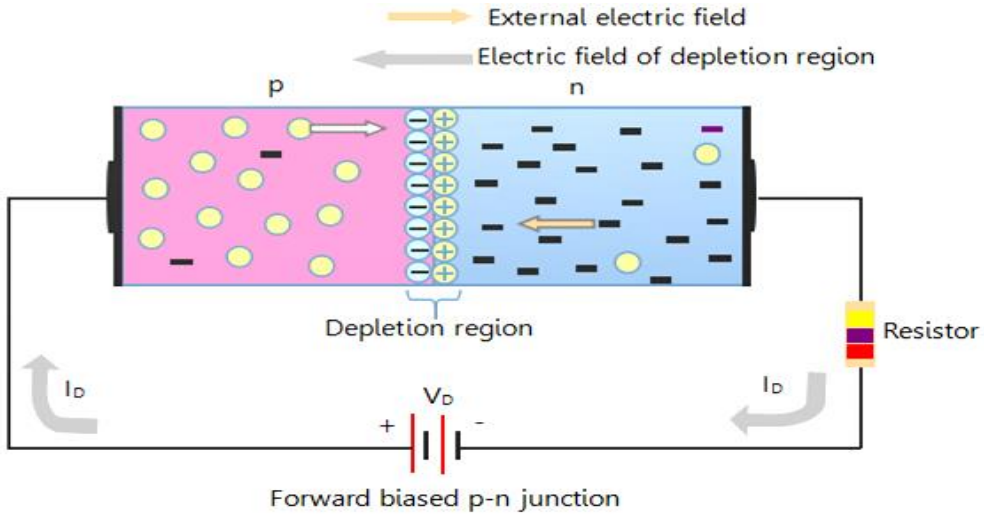


Figure: Forward biased P-N Junction with flow of charge carriers with resistor.

In a reverse-biased PN junction (VD < 0V), the positive terminal is connected to the N-type material, and the negative terminal is connected to the P-type material.

This causes free electrons in the N-region to move toward the positive terminal, leaving behind more positive ions in the depletion region. Similarly, more negative ions are left behind in the P-region.As a result, the depletion region becomes wider, making it harder for current to flow.

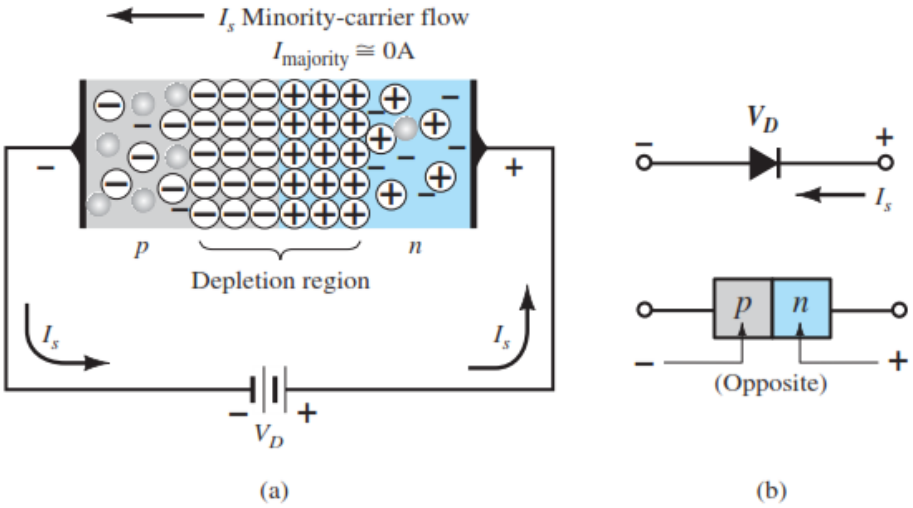


Figure: Reverse-biased P-N Junction: (a) internal distribution of charge under reverse-bias conditions; (b) reverse-bias polarity and direction of reverse saturation current.

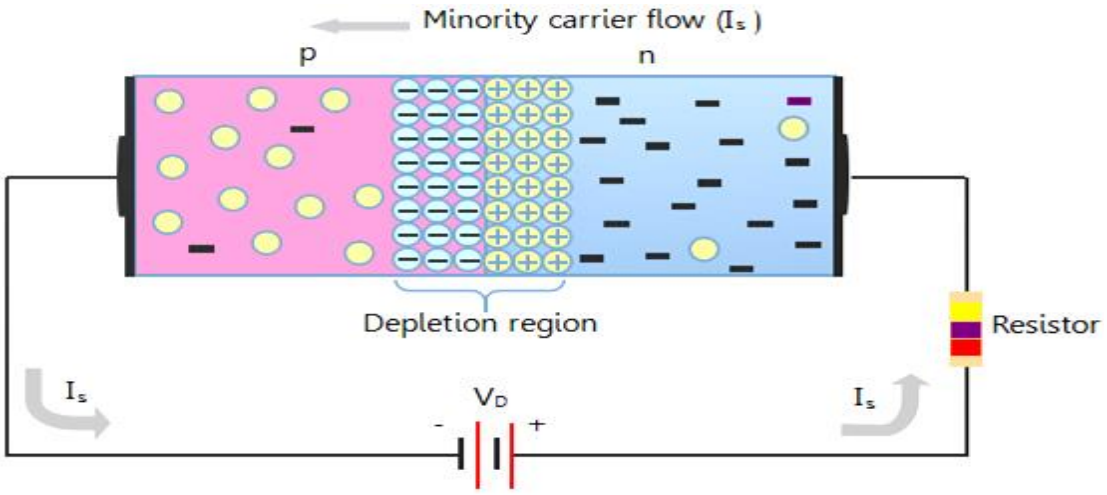


Figure 1.13: Reverse-biased P-N Junction with resistor

In a reverse-biased PN junction, the depletion region widens, blocking majority carriers while allowing minority carriers to flow, resulting in a small reverse saturation current (Is) in the µA or nA range. This current remains nearly constant despite increasing reverse voltage. If the reverse voltage is too high, breakdown (avalanche effect) occurs, useful in voltage stabilization with Zener diodes. Reverse current increases with leakage currents, carrier generation, and temperature, doubling for every 10°C rise.

CLASS-2

Diode act as a Rectifier

A PN junction diode is a polarity-sensitive two-terminal device.

- In forward bias, it conducts with no resistance (ON state).
- In reverse bias, it blocks current (OFF state).

An ideal diode works like a switch, acting as closed (ON) in forward bias and open (OFF) in reverse bias, with zero resistance forward and infinite resistance reverse.

V-I Characteristics:

The V-I characteristics of a PN diode show:

- Forward Bias: Conducts after cut-in voltage (0.7V for silicon, 0.3V for germanium), then current rises exponentially.
- Reverse Bias: Allows only a small leakage current (Is), acting as an open switch.
- Breakdown Region: Large reverse current flows if voltage exceeds breakdown voltage. Zener breakdown occurs below 5V, avalanche breakdown at higher voltages.

The curve shows a sharp current rise in forward bias and minimal current in reverse bias until breakdown.

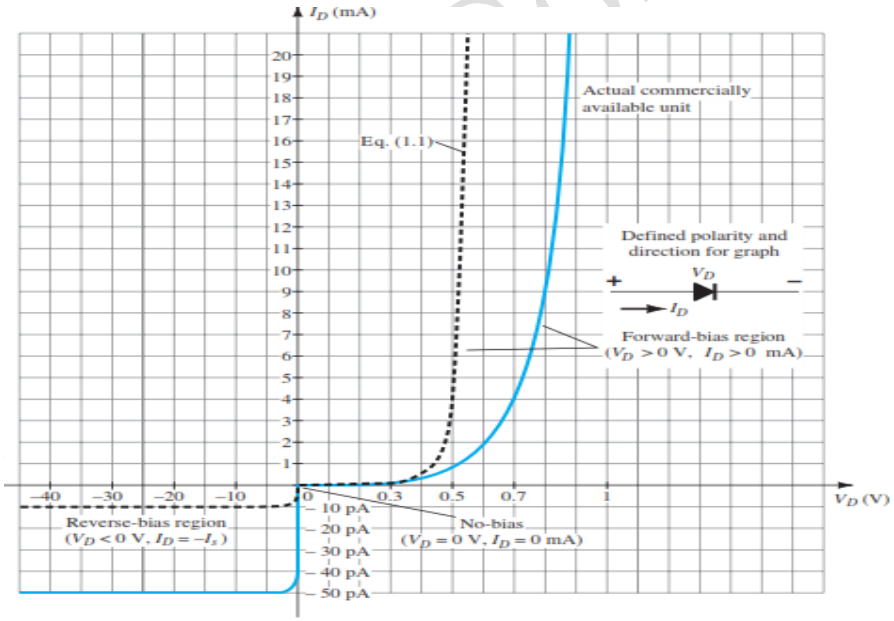


Figure: Silicon semiconductor Diode Characteristics

Temperature Dependence on V-I Characteristics:

Temperature affects diode performance:

- In **forward bias**, increasing temperature (**20°C to 100°C**) **reduces** the voltage by **0.2V**.
- In **reverse bias**, the **reverse current doubles** for every **10°C rise**.
- **Lower temperatures** have the **opposite effect**.

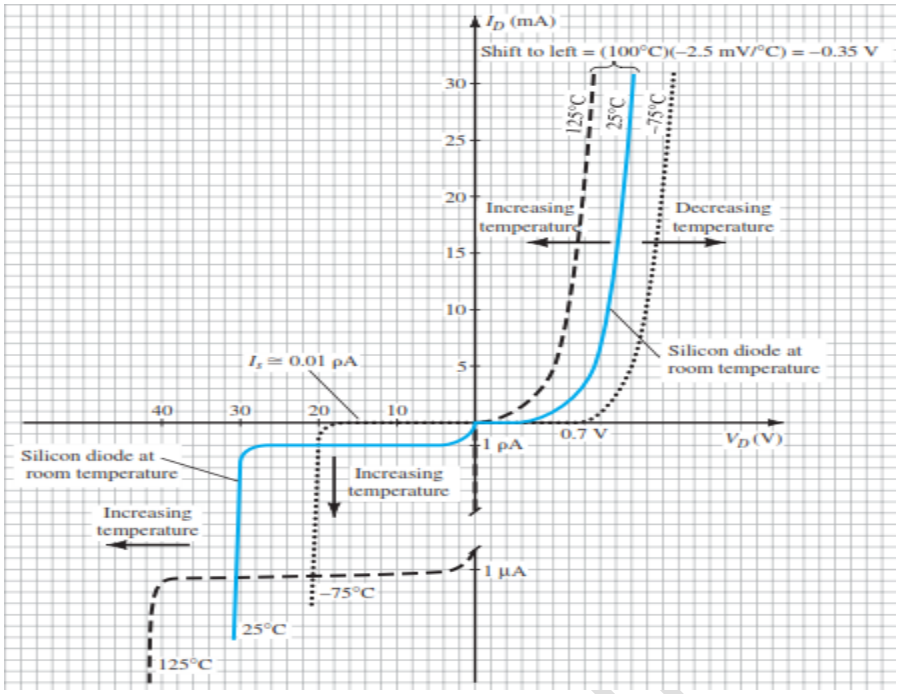


Figure: Variation in Si diode characteristics with temperature change.

Germanium diodes have higher leakage current than silicon diodes, rising from 1–2 µA at 25°C to 100 µA–0.1 mA at 100°C. Silicon diodes have much lower leakage, making them better for high temperatures and providing a superior open-circuit equivalent in reverse bias. Higher leakage at increased temperatures lowers threshold voltage, making forward behavior more ideal. Silicon diodes are preferred in modern designs for their stability.

CLASS-3

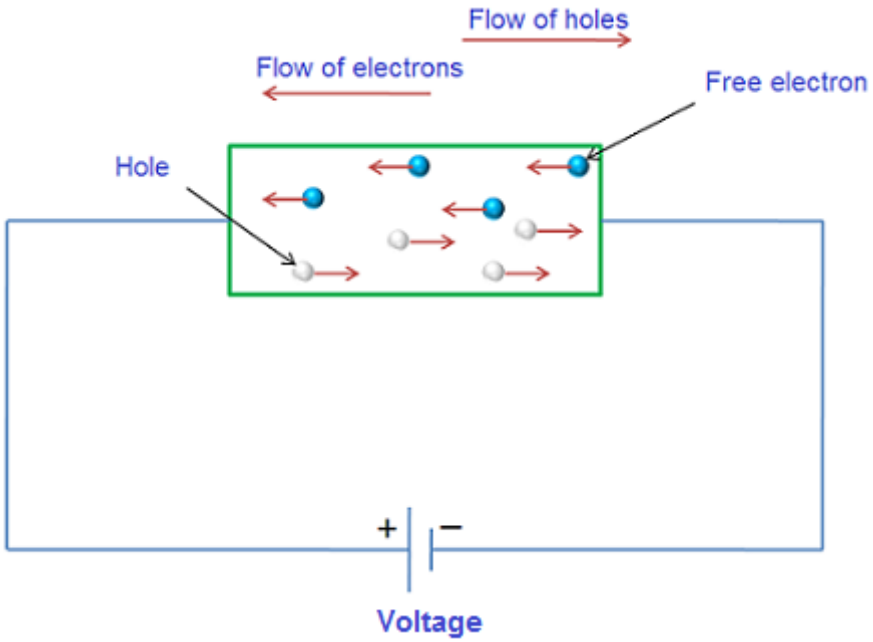
Current Components in PN junction Diode :

Drift current

Drift current is the flow of charge carriers due to an applied voltage or electric field in a semiconductor.

- Electrons (negative) move toward the positive terminal.
- Holes (positive) move toward the negative terminal.

This happens because opposite charges attract and like charges repel.



In a semiconductor, electrons move toward the positive terminal but change direction due to collisions with atoms. Despite random motion, applied voltage causes a net drift toward the positive terminal. The average velocity gained due to this is called drift velocity.

The drift velocity of electrons is given by

$$V_n = \mu_n E$$

The drift velocity of holes is given by

$$V_p = \mu_p E$$

Where v_n = drift velocity of electrons
v_p = drift velocity of holes
μ_n = mobility of electrons
μ_p = mobility of holes
E = applied electric field

The drift current density due to free electrons is given by

$$J_n = e n \mu_n E$$

and the drift current density due to holes is given by

$$J_p = e p \mu_p E$$

Where J_n = drift current density due to electrons
J_p = drift current density due to holes
e = charge of an electron = 1.602×10^{-19} Coulombs (C).
n = number of electrons
p = number of holes

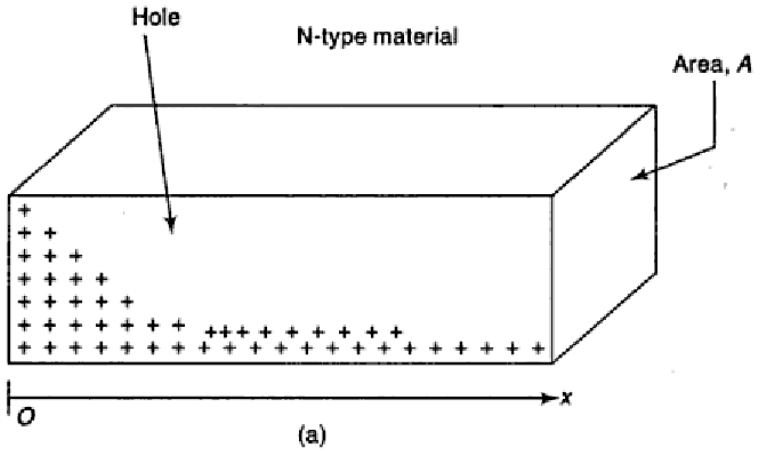
Then the total drift current density is

$$J = J_n + J_p$$
$$= e n \mu_n E + e p \mu_p E$$
$$J = e (n\mu_n + p\mu_p) E$$

Diffusion current

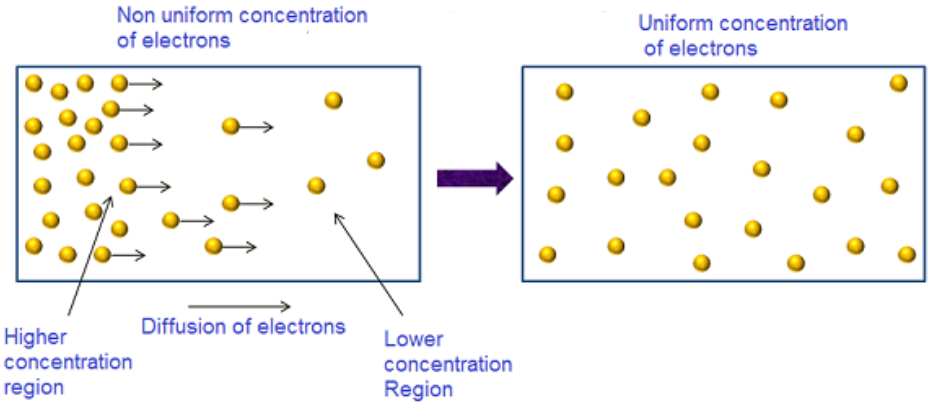
Diffusion is the movement of charge carriers (electrons or holes) from a high concentration region to a low concentration region in a non-uniformly doped semiconductor.

- High concentration region → More electrons
- Low concentration region → Fewer electrons
- Diffusion current is the current caused by this movement.



In a non-uniformly doped n-type semiconductor, more electrons are on the left side than on the right side.

- Higher electron concentration on the left causes repulsion among electrons.
- This leads to electron movement toward the right side where the concentration is lower.



Electrons move to balance concentration, creating diffusion current, which also occurs in p-type semiconductors. Both drift and diffusion currents exist:

- Diffusion Current: No external voltage needed; absent in conductors.
- Direction: Can align or oppose drift current.
- Concentration Gradient: Higher gradient → Higher diffusion current density; Lower gradient → Lower density.

$$J_n \propto \frac{dn}{dx}$$

The concentration gradient for p-type semiconductor is given by

$$J_p \propto \frac{dp}{dx}$$

Where

J_n =diffusion current density due to electrons

J_p = diffusion current density due to holes

Diffusion current density

The diffusion current density due to electrons is given by

$$\boldsymbol{J_n = +eD_n \frac{dn}{dx}}$$

Where D_n is the diffusion coefficient of electrons

The diffusion current density due to holes is given by

$$J_p = -eD_p \frac{dp}{dx}$$

Where D_p is the diffusion coefficient of holes

The total current density due to electrons is the sum of drift and diffusion currents.

J_n = Drift current + Diffusion current

$$J_n = e n \mu_n E + eD_n \frac{dn}{dx}$$

The total current density due to holes is the sum of drift and diffusion currents.

J_p = Drift current + Diffusion current

$$J_p = e n \mu_p E - eD_p \frac{dp}{dx}$$

The total current density due to electrons and holes is given by

$J = J_n + J_p$

The following figure shows a P-N Junction with a forward bias by an external voltage V as shown in Figure 1.15a. Due to the applied voltage, there exists a potential gradient in P and N materials.

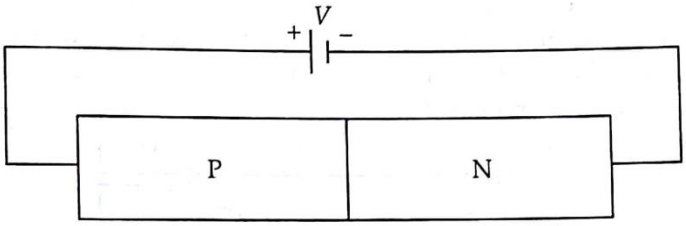


Figure: PN Diode by an external voltage V.

Holes from the P-region and electrons from the N-region drift toward the junction.

- Holes entering the N-region become minority carriers.
- Electrons entering the P-region become minority carriers.
- These minority carriers diffuse away from the junction exponentially with distance.

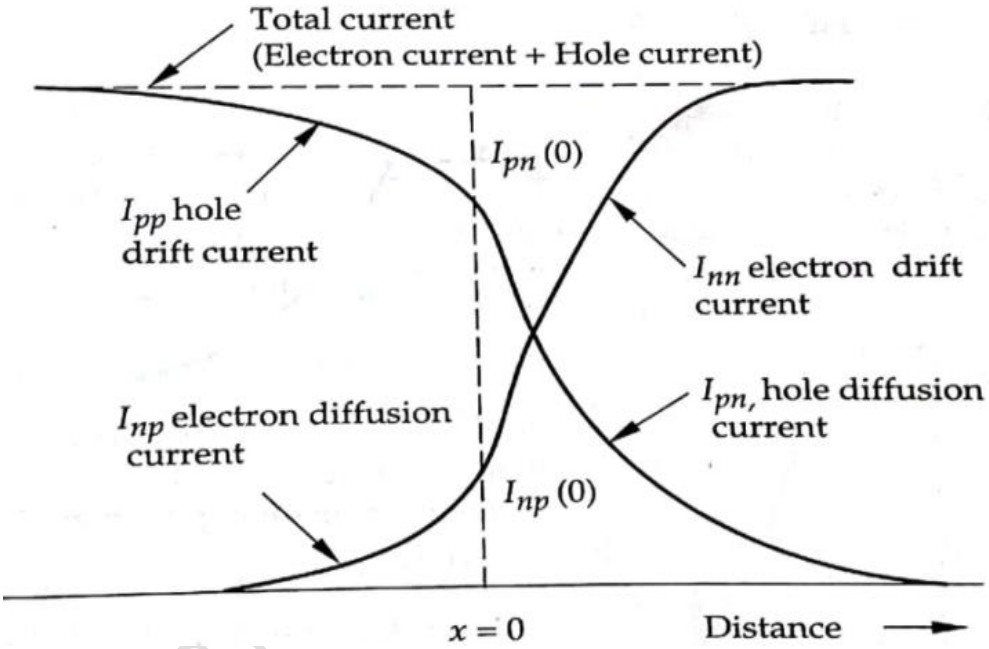


Figure: Current components in forward-biased unsymmetrical junction.

Current Components:

$I_{pn}(x)$ = hole current in N material.

$I_{pn}(0)$ = hole current at junction (x=0)

$I_{np}(x)$ = electron current in P material.

$I_{np}(0)$ = electron current at junction (x=0)

Thus the total current I at junction is given by

$I = I_{pn}(0) + I_{np}(0)$

The majority (electron) current I_{nn} is given by $I_{nn}(x) = I - I_{pn}(x)$

The majority (hole) current I_{pp} is given by $I_{pp}(x) = I - I_{np}(x)$

Quantitative Theory of PN Diode currents

Using quantitative theory, we can derive the total current as a function of the applied voltage.

- In forward bias, holes are injected from the P-side into the N-material.

- The hole concentration in the N-side of the diode decreases exponentially with distance, as shown in the figure.

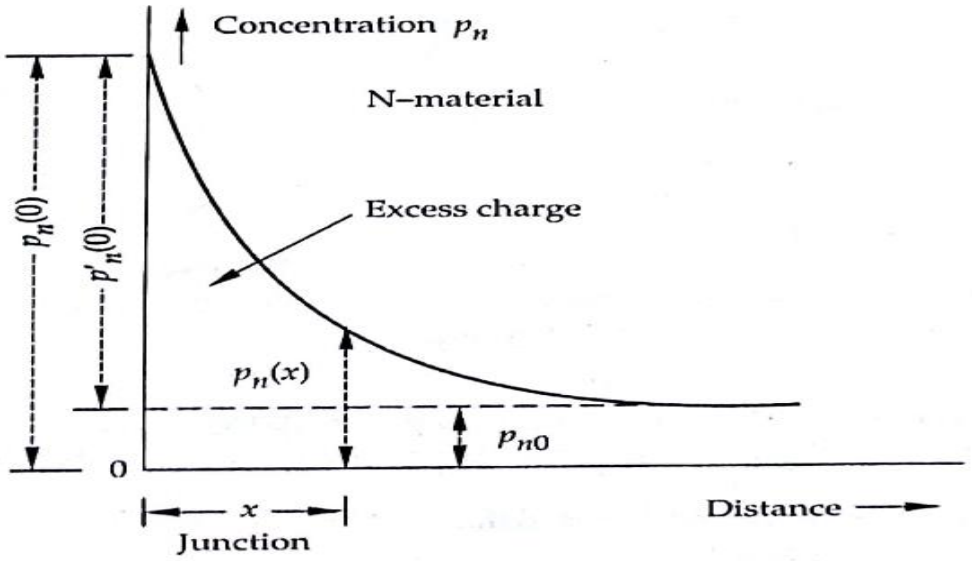


Figure: 1.15c Graph between Concentration and Distance

The hole concentration in N material is given by

$$p_n(x) = p_{n0} + p'_n(0)e^{-x/L_p}$$

whereas x=0

$$p_n(0) = p_{n0} + p'_n(0)$$

Where p_{n_0} = Thermal equilibrium concentration

L_p = diffusion length of holes in N-material

X = distance from the junction where concentration is considered.

$$p'_n(0) = p_n(0) - p_{n0}$$

Diode resistance:

DC Resistance: In a diode circuit with DC voltage, the operating point stays constant. It is given by RD=VD/Id

- Characteristics: Higher at the knee, lower in the steep rise region.
- Reverse Bias: Very high resistance.
- Measurement: Ohmmeters use a small constant current.
- Trend: Higher current → Lower resistance.
- Typical Range: 10Ω to 80Ω in the active region.

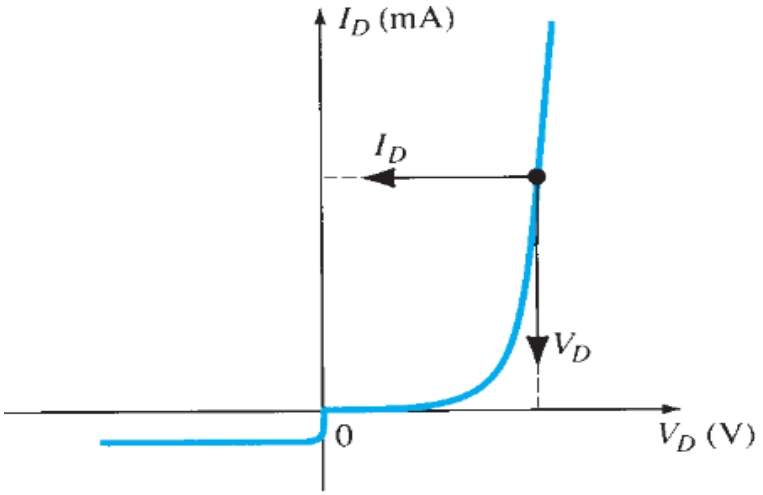


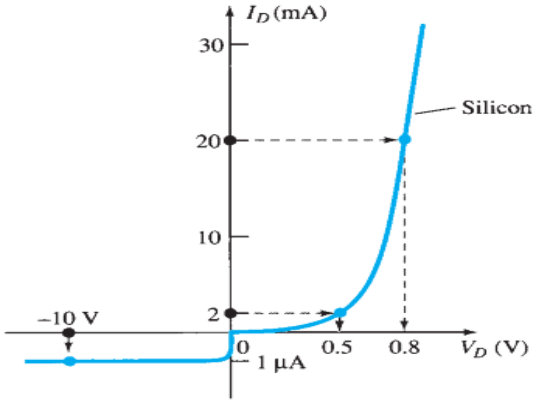
Figure 1.18a Determining the dc resistance of a diode at a particular operating point.

Problem 2 Determine the dc resistance levels for the diode of following figure. at

a.I_D= 2 mA (low level)

b.I_D=20 mA (high level)

c. V_D=10 V (reverse-biased)



a. At I_D = 2 mA, V_D =0.5 V (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{0.5\ V}{2mV} = \mathbf{250\Omega}$$

b. At I_D = 20 mA, V_D =0.8 V (from the curve)

$$R_D = \frac{V_D}{I_D} = \frac{0.8\ V}{20mV} = \mathbf{40\Omega}$$

c. At V_D = -10V, I_D = -I_s = -1 μA (from the curve) and

$R_D = \frac{V_D}{I_D} = \frac{10\ V}{1\ \mu A} = \mathbf{10M\ \Omega}$

- DC Resistance: Remains constant near the operating point.
- AC Signal: Shifts the operating point, changing current and voltage.
- Without AC: Diode stays at a fixed Q-point (steady state) set by DC voltage.
- Q-point: Stands for "quiescent" (unchanging).

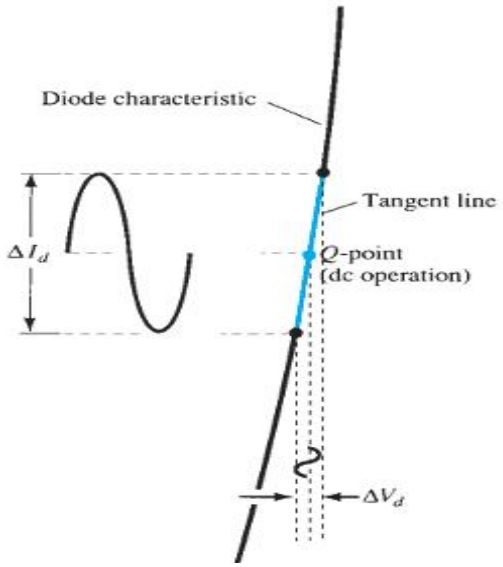


Figure :Defining the Dynamic or ac resistance

A tangent at the Q-point shows voltage and current changes, used to find AC resistance. For accuracy:

- Keep ΔV and ΔI small.
- Ensure changes are symmetrical around the Q-point.

Formula: $\boxed{r_d = \frac{\Delta V_d}{\Delta I_d}}$

where Δ signifies a finite change in the quantity

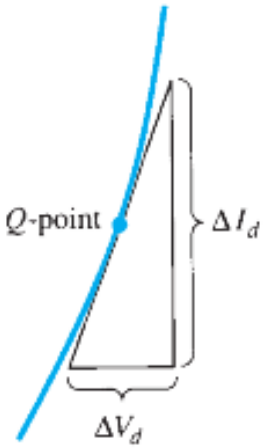


Figure :Determining the ac resistance at a Q – point.

dynamic resistance is determined as $r_f = \frac{\Delta V}{\Delta I}$.

The derivative of a function at a point is equal to the slope of the tangent line drawn at the point. The Schockley's equation for the forward and reverse-bias regions is defined by

$$I = I_o (e^{V/\eta V_T} - 1)$$

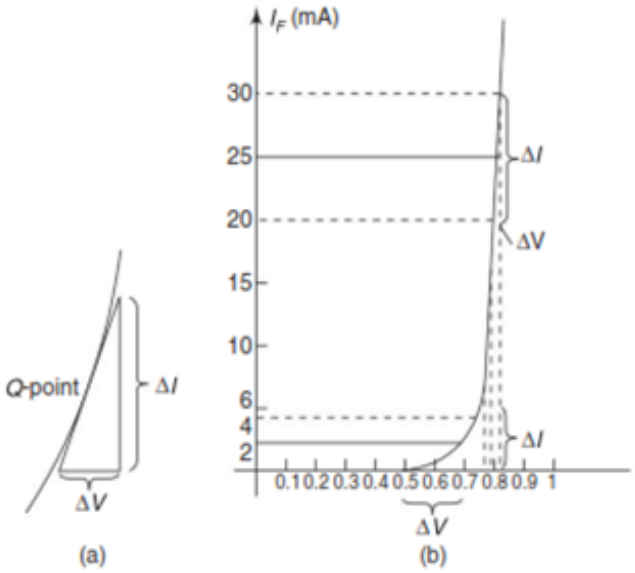
Taking the derivative of the above equation w.r.t. the applied voltage, V, we get

$$\frac{dI}{dV} = \frac{d}{dV}[I_o (e^{V/\eta V_T} - 1)]$$

$$= I_o \left[\frac{1}{\eta V_T} \cdot e^{V/\eta V_T}\right]$$

$$= \frac{I_o e^{V/\eta V_T}}{\eta V_T}$$

$$= \frac{I + I_o}{\eta V_T}$$



Dynamic resistance

Generally, $I >> I_o$ in the vertical-slope section of the characteristics. Therefore,

$$\frac{dI}{dV} \cong \frac{I}{\eta V_T}$$

Therefore, $$\frac{dV}{dI} = r_f = \frac{\eta V_T}{I}$$

CLASS-4

Diode capacitance:

Transition Capacitance (CTC_T): In reverse bias, majority carriers leave the junction, widening the depletion region. The immobile ions act as capacitor plates, creating capacitance. Formula:

$$C_T = \left|\frac{dQ}{dV}\right|$$

where dQ is the increase in charge caused by a change in voltage dV. A change in voltage dV in a time dt will result in a current $I = dQ/dt$ given by

$$I = C_T \frac{dV}{dt}$$

Therefore, C_T is important while considering a diode or a transistor as a circuit element. The quantity C_T is called the transition, space-charge, barrier or depletion region capacitance.

Therefore, $$C_T = \frac{\varepsilon A}{W}$$

Here, ε is the permittivity of the material, A the cross-sectional area of the junction and W is the width of the depletion layer over which the ions are uncovered. The depletion width, W, is given by

$$W = \left[\frac{2\varepsilon_o \varepsilon_r (V_o - V)}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)\right]^{1/2}$$

where V is the applied voltage and V_o is the barrier potential, or the contact potential.

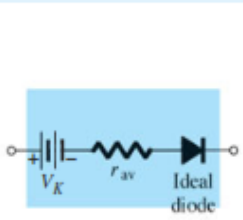
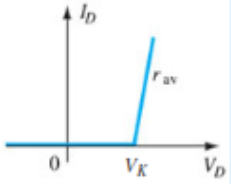
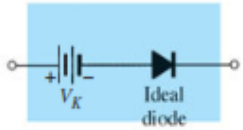
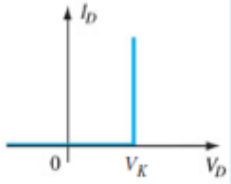
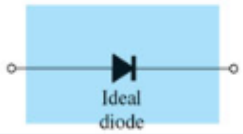
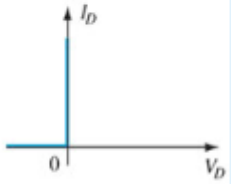
Diffusion Capacitance (C_D)

The capacitance that exists in a forward-biased junction is called a diffusion or storage capacitance (C_D), whose value is usually much larger than C_T, which exists in a reverse-biased junction. This is also defined as the rate of change of injected charge with applied voltage, i.e., $C_D = \frac{dQ}{dV}$, where dQ represents the change in the number of minority carriers stored outside the depletion region when a change in voltage across the diode, dV, is applied.

Piece-Wise Linear Model

An equivalent circuit represents a device's behaviour in a specific operating region. Replacing the actual device with its equivalent circuit allows for standard circuit analysis without significantly altering the system's behaviour.

Diode Equivalent Circuits (Models)

Type	Conditions	Model	Characteristics
Piecewise-linear model			
Simplified model	$R_{network} \gg r_{av}$		
Ideal device	$R_{network} \gg r_{av}$ $E_{network} \gg V_K$		

CLASS-5

Analyzing the Diode Current Equation:

We know that diffusion hole current density in N-side is given by

$$J_p = -QD_p \frac{dp}{dx}$$

$$\frac{I_p}{A} = -QD_p \frac{dp}{dx}$$

$$I_p = -QAD_p \frac{dp}{dx}$$

$$\mathrm{I}_{pn}(x) = -QAD_p \frac{dp_n(x)}{dx}$$

$$\mathrm{I}_{pn}(x) = -QAD_p \frac{d}{dx}\left(p_{n0} + p'_n(0)e^{-x/L_p}\right)$$

$$\mathrm{I}_{pn}(x) = -QAD_p p'_n(0)e^{-x/L_p}\left(\frac{-1}{L_p}\right)$$

$$\mathrm{I}_{pn}(x) = \frac{QAD_p p'_n(0)e^{-x/L_p}}{L_p}$$

At junction i.e., *x= 0*

$$\mathrm{I}_{pn}(0) = \frac{QAD_p p'_n(0)}{L_p}$$

where as $p'_n(0) = p_n(0) - p_{n0}$

$$\mathrm{I}_{pn}(0) = \frac{QAD_p(p_n(0) - p_{n0})}{L_p}$$

Using Boltzmann relationship of Kinetic theory of gases, it can be established that

$$p_n(0) = p_{n_0} e^{V/V_T}$$

$$\mathrm{I}_{pn}(0) = \frac{QAD_p\left(p_{n_0}e^{V/V_T} - p_{n0}\right)}{L_p}$$

Diffusion Hole currentin N-side is

$$I_{pn}(0) = \frac{QAD_p p_{n_0}\left(e^{V/V_T} - 1\right)}{L_p}$$

Diffusion Electron current in P-side is

$$I_{np}(0) = \frac{QAD_n n_{p_0}\left(e^{V/V_T} - 1\right)}{L_n}$$

From the mass-action law,

$$p_{n_0} = \frac{n_i^2}{N_D}$$

$$n_{p_0} = \frac{n_i^2}{N_A}$$

$$I_{pn}(0) = \frac{QAD_p n_i^2\left(e^{V/V_T} - 1\right)}{N_D L_p}$$

$$I_{np}(0) = \frac{QAD_n n_i^2\left(e^{V/V_T} - 1\right)}{N_A L_n}$$

Total Diode Current

The total diode current I at x = 0 is given by

$I_{pn}(0)$ = current caused by holes entering N – region

$I_{np}(0)$ = current caused by electrons entering P – region

$$I = I_{pn}(0) + I_{np}(0)$$

$$I = \frac{QAD_p n_i^2\left(e^{V/V_T} - 1\right)}{N_D L_p} + \frac{QAD_n n_i^2\left(e^{V/V_T} - 1\right)}{N_A L_n}$$

$$I = QAn_i^2\left[\frac{D_p}{N_D L_p} + \frac{D_n}{N_A L_n}\right]\left(e^{V/V_T} - 1\right)$$

$$\boxed{I = I_0\left(e^{V/V_T} - 1\right),}$$

Where as $I_0 = QAn_i^2\left[\frac{D_p}{N_D L_p} + \frac{D_n}{N_A L_n}\right]$

This is known as **Law of Junction**.

Diode CurrentEquation :

In solid-state physics, the behavior of a semiconductor diode in both forward and reverse bias is accurately described by **Shockley's equation**.

$$\boldsymbol{I_D = I_0(e^{V_D/\eta V_T} - 1)}$$

I0 is the reverse saturation current, VD is the forward-bias voltage, and η is the ideality factor, ranging from 1 to 2 depending on conditions, with n = 1 assumed unless stated otherwise. VT is the thermal voltage.

$$V_T = \frac{kT_K}{q}$$

Where k is Boltzmann's constant= 1.38 x 10^{-23} J/K

T_K is the absolute temperature in kelvins = 273 + the temperature in ^oC

q is the magnitude of electronic charge = 1.6 X10^{-19}c

Problem 1 At a temperature of 27°C (common temperature for components in an enclosed operating system), determine the thermal voltage V_T

Solution:

$$T = 273 + °c = 273 + 27 = 300K$$

$$V_T = \frac{kT_k}{q} = \frac{\left(1.38 \times \frac{10^{-23}J}{K}\right)(300K)}{1.6 \times 10^{-19}C}$$

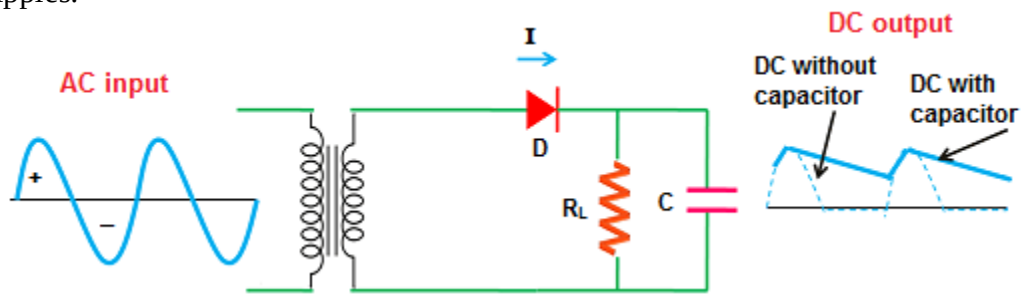
$$= 0.0258V = 25.875mV \cong 26mV$$

The thermal voltage will become an important parameter in the analysis to follow in this chapter and a number of those to follow.

CLASS-6

Quantitative Analysis of Half-wave and Full-wave Rectifiers With and Without Filters

A half-wave rectifier converts AC to DC using a diode. During the positive half-cycle, the diode is forward biased, allowing current to flow, while the negative half-cycle blocks current. The load resistor consumes the DC output, preventing excessive current. In an ideal diode, no negative current flows. A capacitor filter smooths the pulsating DC into steady DC by reducing ripples.



D = Diode
C = Capacitor (Filter)
R_L = Load resistor
I = Current

Half wave rectifier with filter capacitor

Analysis:

In the analysis of a HWR, the following parameters are to be analyzed.

1. DC output current
2. DC Output voltage
3. R.M.S. Current
4. R.M.S. Voltage
5. Rectifier Efficiency (η)
6. Ripple Factor ()
7. Peak Factor
8. % Regulation
9. Transformer Utilization Factor (TUF)
10. Form factor
11. o/p Frequency
12. PIV

Derivations of Characteristics of Rectifiers:

i. Peak Inverse Voltage:

It is the maximum voltage that the rectifying diode has to withstand, when it is reverse biased. The peak inverse voltage (PIV) rating of a diode is of the primary importance in the design of rectification systems.

$$PIV = V_{Smax}$$

ii. Peak Current:

$$I_{max} = \frac{V_{Smax}}{R_F + R_L}$$

iii. Average Output Voltage

The average or dc value of output current is given as

$V_0 = V_m \sin\acute{\omega}t \quad 0 \leq \acute{\omega}t \leq \pi$

$V_0 = 0 \quad \pi \leq \acute{\omega}t \leq 2\pi$

$$V_{ave} = \frac{\int_0^{2\pi} V_0 d(\omega t)}{2\pi - 0}$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin\omega t d(\omega t) + \int_0^{2\pi} 0(\omega t)\right]$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin\omega t d(\omega t)\right]$$

$$= \frac{V_m}{2\pi}[-\cos\omega t d(\omega t)]_0^{\pi}$$

$$= \frac{V_m}{2\pi}[-\cos\pi - (-\cos 0)]$$

$$= \frac{V_m}{2\pi}[-(-1) - (-1)]$$

$$= \frac{V_m}{2\pi}[2]$$

$$V_{ave} = \frac{V_m}{\pi}$$

$$V_{ave} = \frac{V_m}{3.14}$$

$$V_{ave} = 0.318 V_m$$

iv. Average Load Current:

$$I_{dc} = \frac{V_{Smax}}{\pi(R_F + R_L)}$$

$$I_{ave} = \frac{V_{ave}}{R}$$

$$= \frac{V_m/\pi}{R}$$

$$I_{ave} = \frac{V_m}{R\pi}$$

$$I_{ave} = \frac{I_m}{\pi}$$

v. RMS Value of Voltage:

RMS Value of current flowing through the diode (or load resistance R_L) is given as

$$V_{rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} v_0^2 d(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} v_{max}^2 \sin^2 \omega t d(\omega t) + \int_{\pi}^{2\pi} 0 d(\omega t)\right]$$

$$= \frac{v_{max}^2}{2\pi}\left[\int_0^{\pi} \sin^2 \omega t d(\omega t)\right]$$

$$= \frac{v_{max}^2}{2\pi}\left[\int_0^{\pi} \frac{1-\cos 2\omega t}{2} d(\omega t)\right]$$

$$= \frac{v_{max}^2}{2\pi}\left[\frac{\omega t}{2}\right]_0^{\pi}$$

$$= \frac{v_{max}^2}{2\pi} \times \frac{\pi}{2}$$

$$V_{rms}^2 = \frac{v_{max}^2}{4}$$

$$v_{rms} = \frac{v_{max}}{2}$$

vi. RMS Value of current:

RMS Value of current flowing through the diode (or load resistance R_L) is given as

$$I_{rms} = \frac{V_{Smax}}{2(R_F + R_L)}$$

$$v_{rms} = I_{rms} R_L$$

If $R_L \gg R_F$

$$I_{rms} = \frac{I_{max}}{2}$$

Form Factor: The form factor defined as the ratio of rms value to average value is given by

$$K_f = \frac{RMS\ value}{Average\ value} = \frac{I_{rms}}{I_{dc}} = \frac{\frac{V_{Smax}}{2(R_F+R_L)}}{\frac{V_{Smax}}{\pi(R_F+R_L)}} = \frac{\pi}{2} = 1.57$$

Peak Factor: The peak factor defined as the ratio of peak value to rms value, is given by

$$K_f = \frac{Peak\ value}{RMS\ value} = \frac{\frac{V_{Smax}}{(R_F+R_L)}}{\frac{V_{Smax}}{2(R_F+R_L)}} = 2$$

Ripple Factor :

The output current has both AC and DC parts. The **ripple factor** measures how much AC is present in the rectified output. It is the ratio of the RMS value of the AC component to the DC component in the output.

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

Efficiency (ŋ):

It is the ratio of d.c output power to the a.c. input power. It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power.

$$\eta = \frac{o/p\ power}{i/p\ power}$$

Transformer Utilization Factor (UTF) :

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the Transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{p_{ac(rated)}}$$

% Regulation:

The variation of the d.c. output voltage as a function of d.c. load current is called regulation. The percentage regulation is defined as

$$\%\,Regulation = \frac{V_{NL} - V_{FL}}{V_{FL}} * 100$$

Advantages of Half-Wave Rectifier:

- Uses fewer components, making it low-cost.
- Simple and easy to build.

Disadvantages of Half-Wave Rectifier:

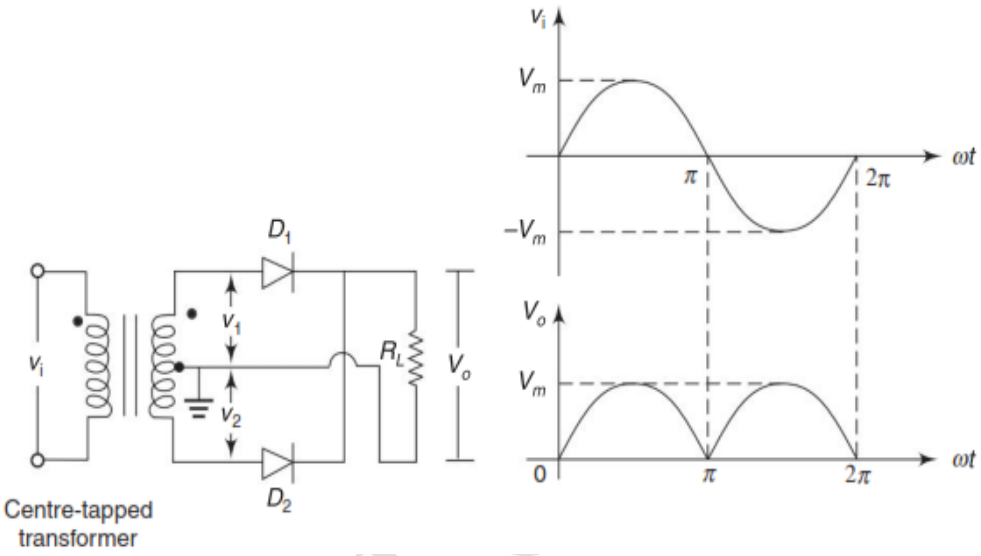
- **Power Loss:** It only allows one half-cycle (positive or negative), wasting the other half. So, nearly half of the input voltage is lost.
- **Pulsating DC:** The output is not a smooth DC but a fluctuating one, which is less useful.
- **Low Output Voltage:** It produces a lower voltage compared to other rectifiers.

CLASS-7

Full Wave Rectifier: (input and output waveforms)

A full-wave rectifier converts AC voltage into a pulsating DC voltage using both half-cycles of the input AC. It uses two diodes—one conducts during the positive half-cycle, and the other conducts during the negative half-cycle. There are two types of full-wave rectifiers:

1. **Full-wave rectifier with a center-tapped transformer**
2. **Bridge rectifier (without a transformer)**



Full-waverectifier

In a full-wave rectifier with a center-tap transformer, during the positive half-cycle, D1 conducts and the voltage across RL equals the input voltage. During the negative half-cycle, D1 is off, D2 conducts, and the voltage across RL remains the same as the input voltage.

Ripple Factor (Γ)

$$\Gamma = \sqrt{\left(\frac{V_{\text{rms}}}{V_{\text{dc}}}\right)^2 - 1}$$

$$V_{\text{dc}} = \frac{1}{\pi}\int_0^{\pi} V_m \sin \omega t \, \mathrm{d}(\omega t)$$

$$= \frac{V_m}{\pi}[-\cos \omega t]_0^{\pi} = \frac{2V_m}{\pi}$$

$$I_{\text{dc}} = \frac{V_{\text{dc}}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi} \text{ and } I_{\text{rms}} = \frac{I_m}{\sqrt{2}}$$

If the diode forward resistance (r_f) and the transformer secondary winding resistance (r_s) are included in the analysis, then

$$V_{dc} = \frac{2V_m}{\pi} - I_{dc}(r_s + r_f)$$

$$I_{dc} = \frac{V_{dc}}{(r_s + r_f) + R_L} = \frac{2V_m}{\pi(r_s + r_f + R_L)}$$

The rms value of the voltage at the load resistance is

$$V_{rms} = \sqrt{\left[\frac{1}{\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t \, d(\omega t)\right]} = \frac{V_m}{\sqrt{2}}$$

Therefore,
$$\Gamma = \sqrt{\left(\frac{V_m/\sqrt{2}}{2V_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.482$$

Efficiency (η) The ratio of dc output power to ac input power is known as rectifier efficiency (η).

$$\eta = \frac{\text{dc output power}}{\text{ac input power}} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{(V_{dc})^2/R_L}{(V_{rms})^2/R_L} = \frac{\left[\frac{2V_m}{\pi}\right]^2}{\left[\frac{V_m}{\sqrt{2}}\right]^2}$$

$$= \frac{8}{\pi^2} = 0.812 = 81.2\%$$

The maximum efficiency of a full-wave rectifier is 81.2%.

Transformer Utilization Factor (TUF) The average TUF in a full-wave rectifying circuit is determined by considering the primary and secondary windings separately and it gives a value of 0.693.

- **Form Factor**

$$\text{Form factor} = \frac{\text{rms value of the output voltage}}{\text{average value of the output voltage}} = \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{\pi}{2\sqrt{2}} = 1.11$$

- **Peak Factor**

$$\text{Peak factor} = \frac{\text{peak value of the output voltage}}{\text{rms value of the output voltage}} = \frac{V_m}{V_m/\sqrt{2}} = \sqrt{2}$$

Zener Diode and its Characteristics

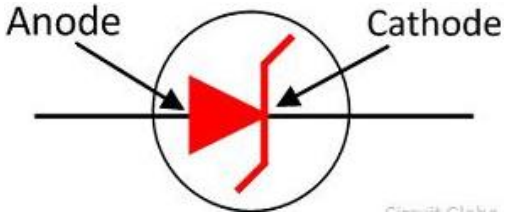


Figure : Symbol of Zener diode

Operation:

Zener Diodes acts like normal p-n junction Diodes under forward biased condition.When forward biased voltage is applied to the zenerDiode it allows electric current in forward direction like a normal Diode as shown in Figure 1.25a.

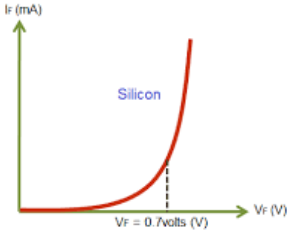


Figure : Forward bias Characteristics of silicon diode and Zener diode

A zener diode operates in the reverse breakdown region, with two types of breakdown: zener and avalanche. In zener breakdown, when the reverse voltage increases, the strong electric field at the depletion region pulls electrons, causing a rapid rise in current near the Zener voltage (below 6V).

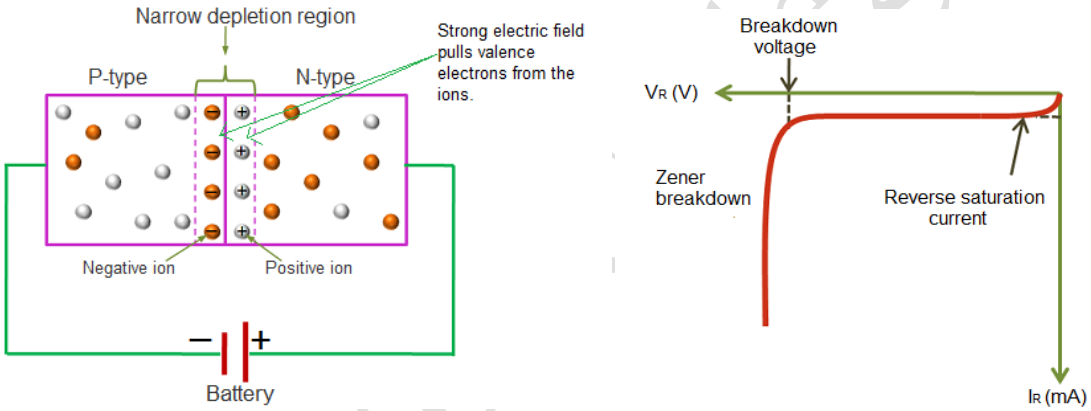


Figure : Reverse bias connection in Zener Diode with Zener breakdown Characteristics

Avalanche breakdown:

Avalanche breakdown happens in both normal and Zener diodes at high reverse voltage.

- High reverse voltage gives free electrons extra energy, making them move faster.
- These fast electrons collide with atoms, knocking off more electrons.
- The new electrons also accelerate and collide, creating even more free electrons.
- This chain reaction causes a sudden rise in current through the diode.

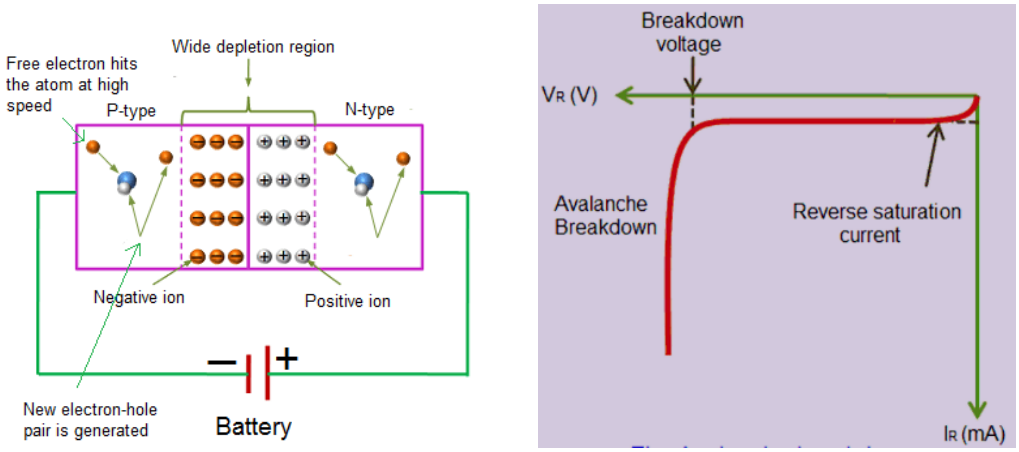


Figure : Reverse bias connection in Zener Diode with Avalanche breakdown Characteristics

A normal diode gets permanently damaged.

V-I Characteristics:

The Zener diode behaves like an ordinary diode in forward bias. When the reverse voltage is less than 6V, zener breakdown occurs. Beyond 6V, avalanche breakdown takes place.

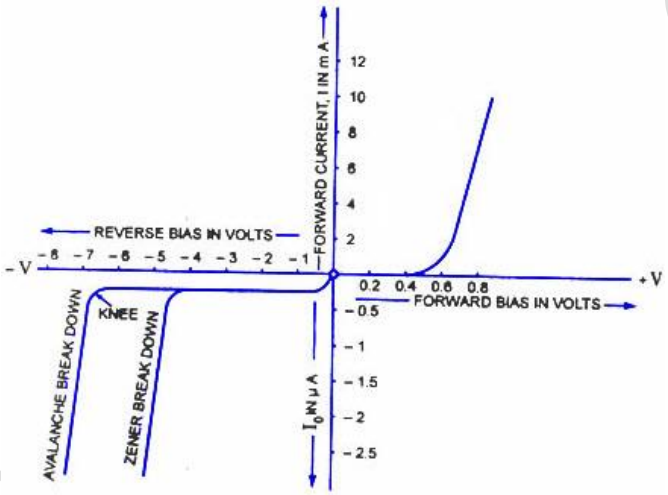


Figure :zener diode Characteristics

CLASS-8

LED:

Light is energy released by atoms in the form of photons, which have energy and momentum but no mass. LEDs, a type of semiconductor diode, emit light when forward biased. They convert electrical energy directly into light, with infrared LEDs used in remote controls.

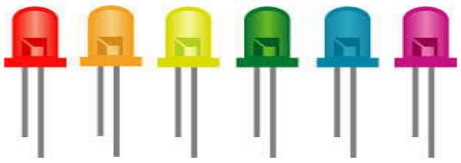


Figure : Different colors of LEDs

When an LED is forward biased, electrons in the conduction band combine with holes in the valence band, emitting light through electroluminescence. Like regular diodes, LEDs only allow current in the forward direction. LEDs use materials like gallium, phosphorus, and arsenic, unlike regular diodes that use silicon or germanium, as these materials emit light rather than heat.

Light Emitting Diode (LED) working:

An LED works only in forward bias. When forward biased, free electrons from the n-side and holes from the p-side move toward the junction. At the junction, electrons recombine with holes in positive ions, releasing energy as light. Similarly, holes from the p-side recombine with electrons in the depletion region.

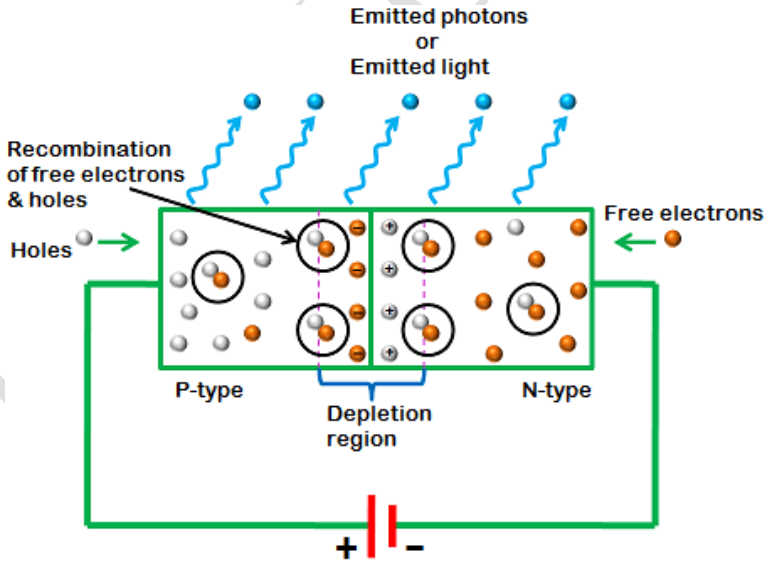


Figure: Biasing of LED

When free electrons and holes recombine in the depletion region, its width decreases, allowing more charge carriers to cross the p-n junction. Some charge carriers cross the junction before recombining. Recombination occurs in the depletion region, p-type, and n-type materials, with free electrons releasing energy as light before recombining with holes. In silicon and germanium diodes, energy mostly turns into heat, emitting little light, while materials like gallium arsenide and gallium phosphide emit bright visible light.

Operation of LED

When voltage is applied, valence electrons gain energy, break free from atoms, and become free electrons, leaving behind holes. The valence band corresponds to the energy range of valence electrons, while the conduction band corresponds to free electrons. Free electrons in the conduction band lose energy as light and recombine with holes, emitting light with each recombination.

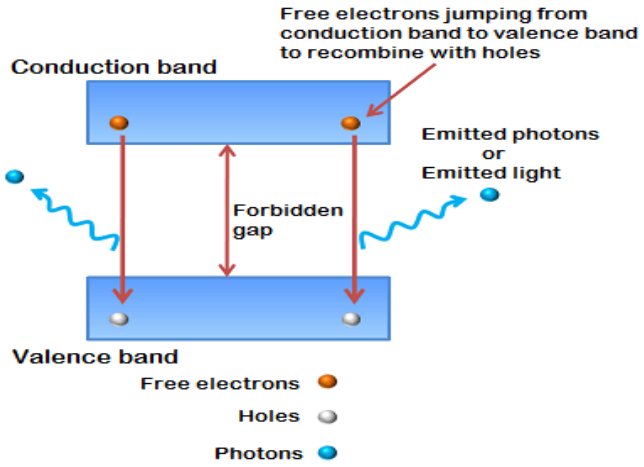


Figure : Process of light emission in LED

The intensity of emitted light in an LED depends on the energy gap between the conduction and valence bands; a larger gap produces brighter light. Brightness also depends on the material and forward current. Efficiency increases with higher current and lower temperature. In forward bias, recombination produces light, but in reverse bias, charge carriers move away, preventing light emission. High reverse voltage can damage the LED. While all diodes emit light, only those with specific materials produce visible light. LEDs can switch on and off in 1 nanosecond.

Light emitting diode (LED) symbol

The symbol of LED is similar to the normal p-n junction diode except that it contains arrows pointing away from the diode indicating that light is being emitted by the diode.

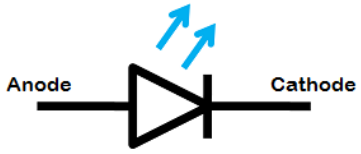


Figure : Symbol of LED

LEDs come in various colors, including orange, yellow, green, and red. The schematic symbol for an LED is the same for all colors, so the color of the light cannot be identified from the symbol. To protect the LED, a resistor (Rs) is placed in series with it, between the voltage source (Vs) and the LED.

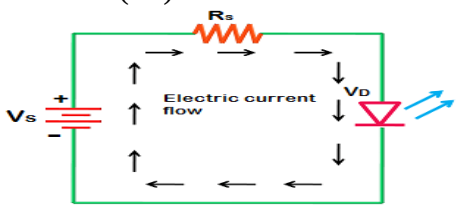


Figure : Current flow in LED circuit.

The current flowing through the LED is mathematically written as

$$I_F = \frac{V_S - V_D}{R_S}$$

Where

IF = Forward current

VS = Source voltage

VD = Voltage drop across LED

RS = Resistor

Voltage Drop:

- LED: 2–3V
- Silicon/Germanium diode: 0.3–0.7V

Output:

- Light output is proportional to forward current.
- More current → More light.

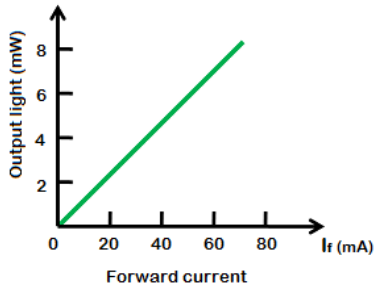


Figure : Characteristics of LED

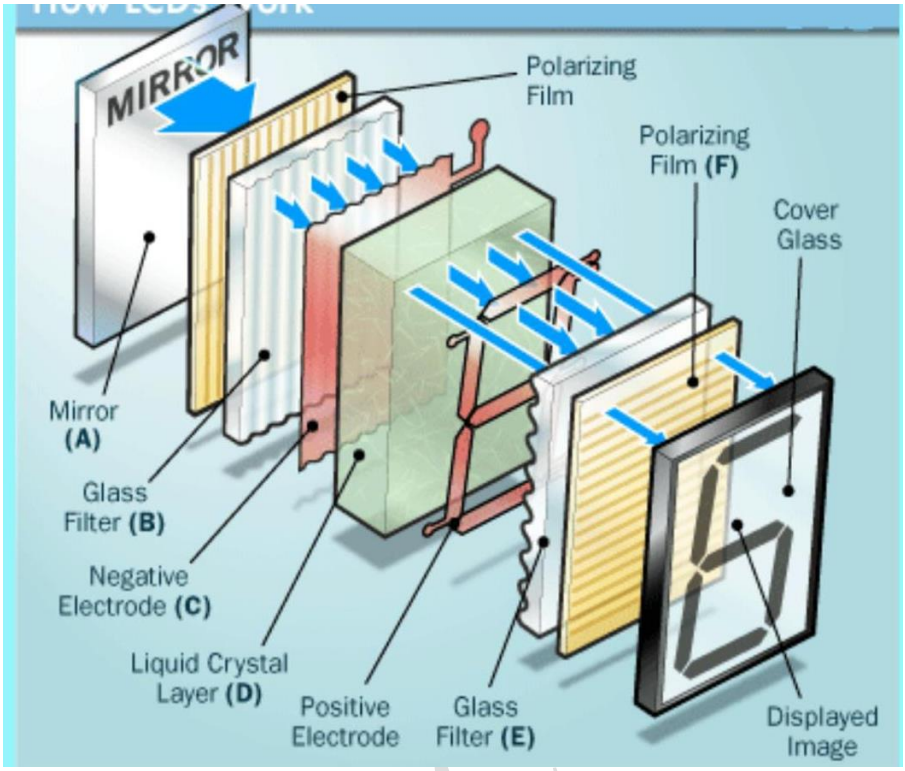
LED Color	Forward Voltage(V) @ 20mA		Dominant wavelength(mm)K @ 20mA	
	Min	Typ	Min	Typ
Red	2.1	2.4	620	630
Yellow	2.1	2.4	580	590
Green	3.4	3.8	520	530
Blue	3.4	3.8	460	465
White	3.4	3.8	6000	6500
Warm- White	3.4	3.8	3000	3500

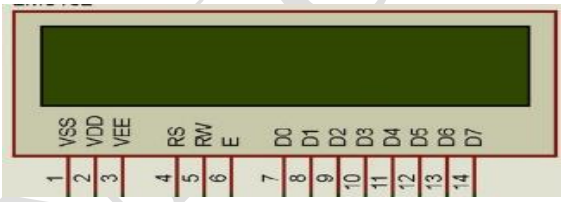
Table : Typical values of LEDs

- Different materials emit different colors of light.
- Gallium arsenide LEDs emit red and infrared light.
- Gallium nitride LEDs emit bright blue light.
- Yttrium aluminium garnet LEDs emit white light.

LCD:

LCDs use liquid crystals for displays, with red, green, and blue subpixels. The screen appears black when off and white when on. They have two layers with polarized filters and electrodes, blocking light instead of emitting it. There are two types of pixel grids: Active Matrix (newer, used in smartphones) and Passive Matrix (older). LCDs rely on liquid crystals and polarized light, with a backlight reflecting images when current is applied.





LCD

List of devices using LCD :

LCDs are used in devices like calculators, TVs, mobile devices, smartphones, laptops, gaming systems, computers, and digital clocks.

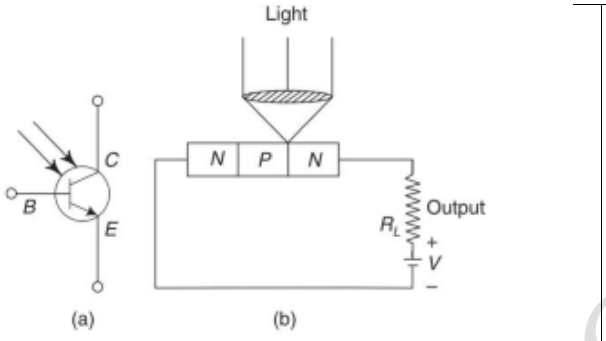
Benefits of LCD:

- Low cost, energy-efficient, and consumes less energy.
- Smaller, thinner, and flexible.
- Offers excellent contrast, brightness, and resolution for clear images.
- Emits less radiation compared to CRT monitors.

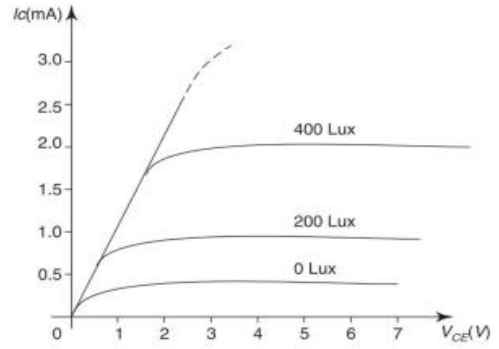
CLASS-9

Photodiode:

- Phototransistor vs. Photodiode: More sensitive than a PN photodiode.
- Photodiode Limitation: Produces low current, requiring amplification for control applications.
- Phototransistor Function: Combines a photodiode and transistor amplifier, allowing more current flow when illuminated.
- Circuit Configuration:
  - Usually NPN, connected in common-emitter (CE) mode with an open base.
  - A lens focuses light on the base-collector junction.
- Leads: Uses only emitter and collector; base current is generated by light on the junction.



NPN phototransistor: (a) Symbol (b) Biasing arrangement



Characteristics of a phototransistor

When there is no radiant excitation, the minority carriers are generated thermally, and the electrons crossing from the base to the collector and the holes crossing from the collector to the base constitute the reverse saturation collector current I_{CO}. With $I_B = 0$, the collector current is given by

$$I_C = (\beta + 1)\, I_{CO}$$

When the light is turned ON, additional minority carriers are photogenerated and the total collector current is

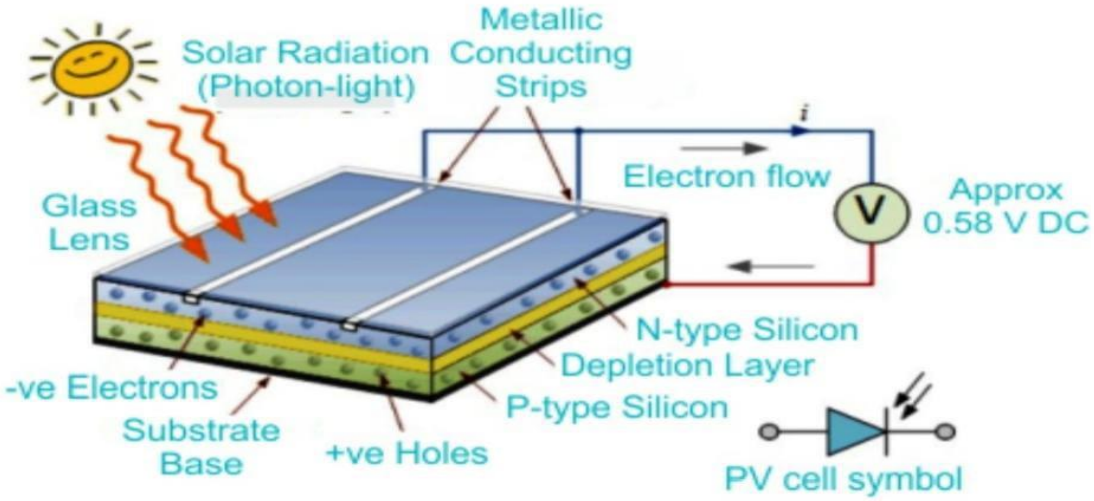
$$I_C = (\beta + 1)(I_{CO} + I_L)$$

where I_L is the reverse saturation current due to the light.

Solar Cell :

A **solar cell** is a special type of **photodiode** designed to convert light energy directly into electrical energy using the **photovoltaic effect**. While it shares some characteristics with regular diodes, it has unique properties and applications, particularly in renewable energy systems.

Solar cells consist of two semiconductor layers with opposite charges. When sunlight hits the cell, it knocks electrons loose, creating an electric flow. The photovoltaic effect generates voltage and current as photons excite electrons, forming electron-hole pairs. The internal electric field at the PN junction separates these charges, with electrons moving to the n-type region and holes to the p-type region, creating a potential difference that allows current to flow when connected to an external load.



A solar cell has multiple layers, with a P-N junction formed by doping silicon with phosphorus (n-type) and boron (p-type). An anti-reflective coating allows more photons to enter, and metallic contacts collect charge carriers. Encapsulation protects the cell.

The I-V characteristics define performance:

- Voc is the maximum voltage with no current.
- Isc is the highest current when shorted.
- Pmax is the point of maximum power output.

$$I = I_{\text{ph}} - I_0 \left[e^{\frac{V+IR_s}{nV_T}} - 1 \right] - \frac{V + IR_s}{R_{sh}}$$

Where:

- I_{ph}: Photocurrent
- I_0: Reverse saturation current
- V_T: Thermal voltage (kT/q)
- n: Ideality factor of the diode
- R_s: Series resistance
- R_{sh}: Shunt resistance

UNIT- 2: Bipolar Junction Transistor (BJT) Characteristics

S. No	Topic Name
1.	The Junction Transistor- Operation
2.	Transistor Current Components
3.	Transistor Current Equation
4.	Transistor configurations
5.	Characteristics of CB, CE and CC Configurations
6.	Comparison CB, CE and CC Configurations
7.	Early Effect, Punch Through/Reach Through
8.	Transistor as an Amplifier
9.	Ebers-Moll model of a transistor
10.	Large Signal, DC and Small Signal CE Values of Current Gain
11.	Typical Transistor-Junction Voltages
12.	Transistor as a Switch
13.	Transistor Switching Times
14.	Maximum Voltage Rating
15	Photo Transistor, UJT

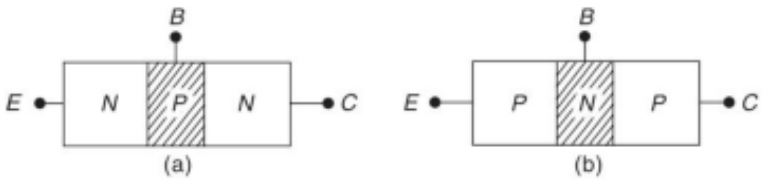
CLASS-10

BJT: Junction Transistor:

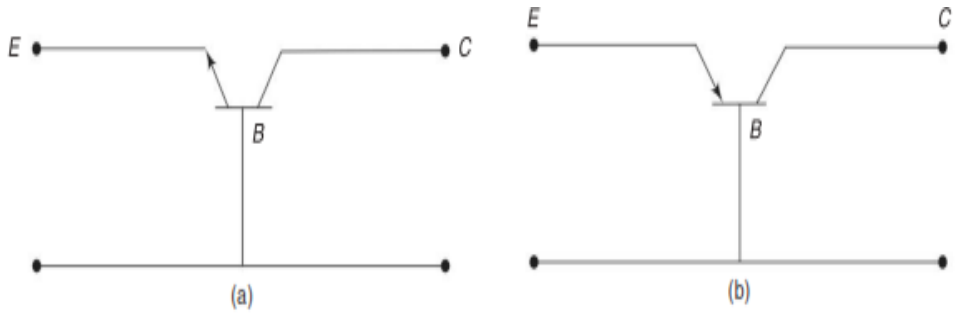
A Bipolar Junction Transistor (BJT) is a three-terminal semiconductor device that operates using both majority and minority carriers, making it bipolar. A solar cell has multiple layers, with a P-N junction formed by doping silicon with phosphorus (n-type) and boron (p-type). An anti-reflective coating allows more photons to enter, and metallic contacts collect charge carriers. Encapsulation protects the cell.

The I-V characteristics define performance:

- Voc is the maximum voltage with no current.
- Isc is the highest current when shorted.
- Pmax is the point of maximum power output.



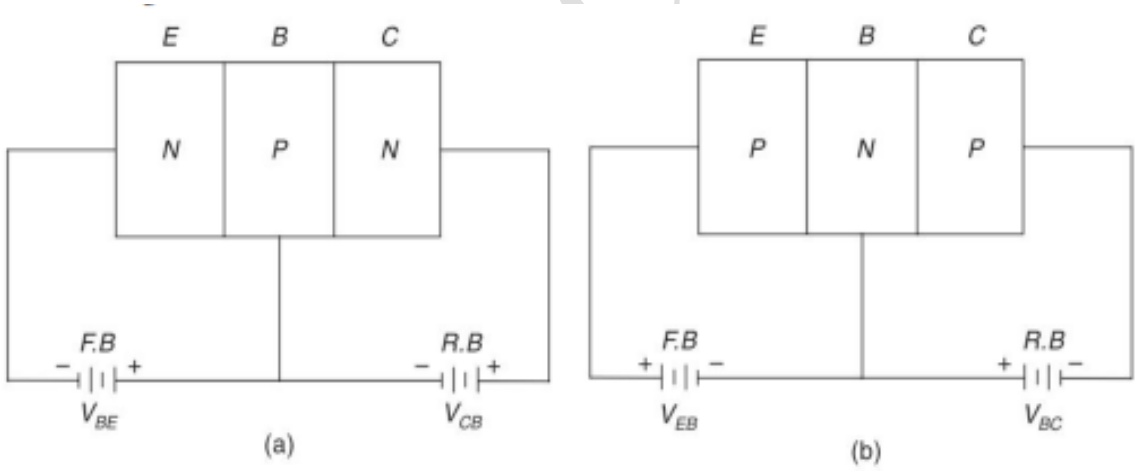
Transistor: (a) NPN (b) PNP



Circuit symbol: (a) NPN transistor (b) PNP transistor

Transistor Biasing

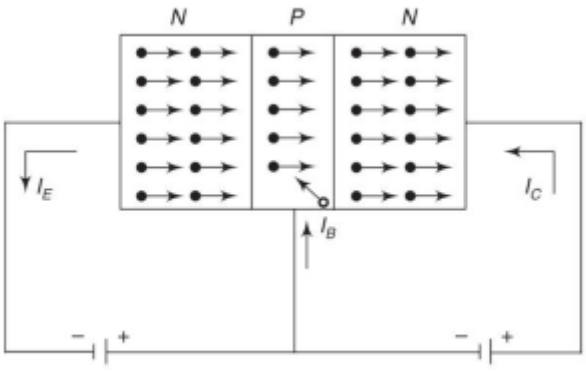
In a Bipolar Junction Transistor (BJT), the emitter-base junction is forward biased, and the collector-base junction is reverse biased. This forward bias allows an emitter current to flow from the emitter to the base. Despite the reverse bias at the collector-base junction, almost the entire emitter current passes through the collector circuit, making the BJT a current-controlled device.



Transistor biasing: (a) NPN transistor (b) PNP transistor

OperationofanNPNTransistor:

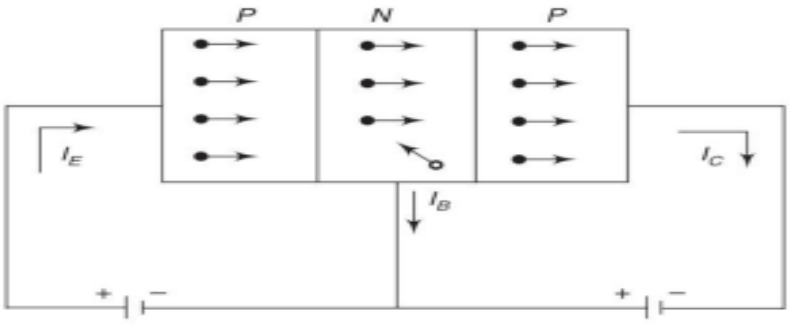
In an NPN transistor, forward bias on the emitter-base junction causes electrons to move from the emitter into the base. Since the base is lightly doped, only a few electrons recombine, creating a small base current (IB). Most electrons (over 95%) cross into the collector, forming the collector current (IC). The total emitter current (IE) is the sum of the base and collector currents: IE = IC + IB.



Current in an NPN transistor

Operation of a PNP Transistor :

In a PNP transistor, forward bias causes holes to move from the emitter to the base. Most holes (over 95%) cross into the collector, creating the collector current (IC), while a small number recombine in the base, forming the base current (IB). The total emitter current (IE) is the sum of the base and collector currents: IE = IC + IB.



Current in a PNP transistor

Transistor current components:

Current Amplification Factor

In a transistor amplifier with ac input signal, the ratio of change in output current to the change in input current is known as the current amplification factor.

In the CB configuration, the current amplification factor, $\alpha = \frac{\Delta I_C}{\Delta I_E}$

In the CE configuration, the current amplification factor, $\beta = \frac{\Delta I_C}{\Delta I_B}$

In the CC configuration, the current amplification factor, $\gamma = \frac{\Delta I_E}{\Delta I_B}$

Relationship between α and β

We know that $\Delta I_E = \Delta I_C + \Delta I_B$

By definition, $\Delta I_C = \alpha \Delta I_E$

Therefore, $\Delta I_E = \alpha \Delta I_E + \Delta I_B$

i.e., $\Delta I_B = \Delta I_E (1 - \alpha)$

Dividing both sides by ΔI_C, we get

$$\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C}(1 - \alpha)$$

Therefore, $$\frac{1}{\beta} = \frac{1}{\alpha}(1 - \alpha)$$

$$\beta = \frac{\alpha}{(1 - \alpha)}$$

Rearranging, we also get $\alpha = \frac{\beta}{(1 + \beta)}$, or $\frac{1}{\alpha} - \frac{1}{\beta} = 1$

Relation among α, β, and γ

In the CC transistor amplifier circuit, I_B is the input current and I_E is the output current.

From Eq. (4.2), $$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Substituting $\Delta I_B = \Delta I_E - \Delta I_C$,

we get $$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator on RHS by ΔI_E, we get

$$\gamma = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1 - \alpha}$$

Therefore, $$\gamma = \frac{1}{1 - \alpha} = (\beta + 1)$$

CLASS-11

Transistor Current Equation :

In the active region of the transistor, the emitter-base junction is forward biased and the collector-base junction is reverse biased. The generalized expression for collector current I_C for collector junction voltage V_C and emitter current I_E is given by

$$I_C = -\alpha I_E + I_{CBO}\left(1 - e^{V_C/V_T}\right)$$

If V_C is negative and $|V_C|$ is very large compared with V_T, then the above equation reduces to

$$I_C = -\alpha I_E + I_{CBO}$$

If V_C, i.e., V_{CB}, is a few volts, then I_C is independent of V_C. Hence, the collector current I_C is determined only by the fraction α of the current I_E flowing in the emitter.

Relation Among I_C, I_B, and I_{CBO}

From Eq. (4.10), we have

$$I_C = -\alpha I_E + I_{CBO}$$

Since I_C and I_E are flowing in opposite directions,

$$I_E = -(I_C + I_B)$$

Therefore,

$$I_C = -\alpha[-(I_C + I_B)] + I_{CBO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C(1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

Since

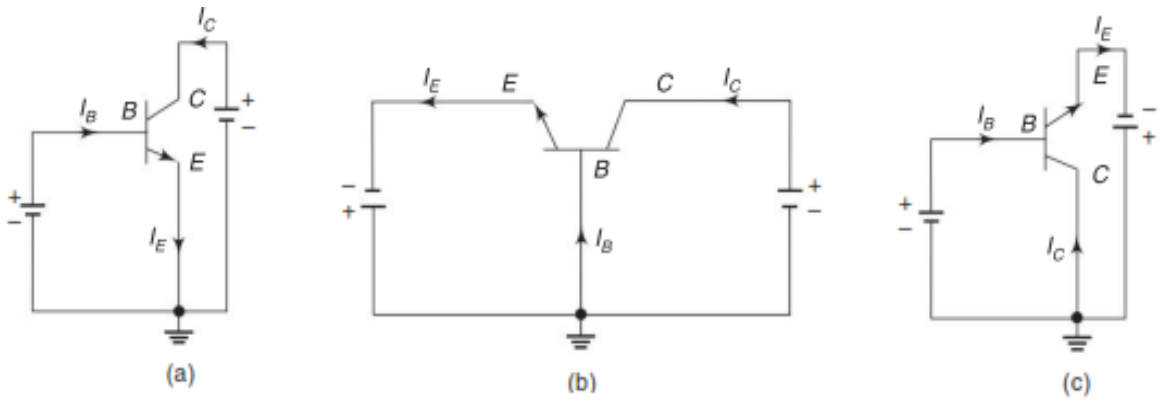
$$\beta = \frac{\alpha}{1-\alpha}$$

the above expression becomes

$$I_C = (1 + \beta) I_{CBO} + \beta I_B$$

Transistor Configurations:

In the Common Base (CB) configuration, also known as the grounded-base configuration, the emitter serves as the input terminal, the collector as the output terminal, and the base as the common terminal.



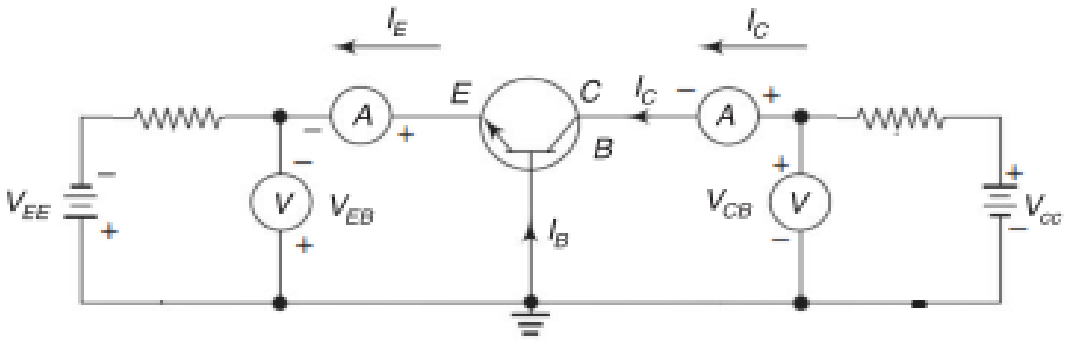
Transistor configuration: (a) Common emitter (b) Common base (c) Common collector

In the Common Emitter (CE) configuration, the base is the input, the collector is the output, and the emitter is common. In the Common Collector (CC) configuration, the base is the input, the emitter is the output, and the collector is common. The supply voltage connections for normal operation of an NPN transistor in these configurations are as shown in the figure.

Characteristics of CB, CE and CC Configurations

Characteristics of transistor in Common Base:

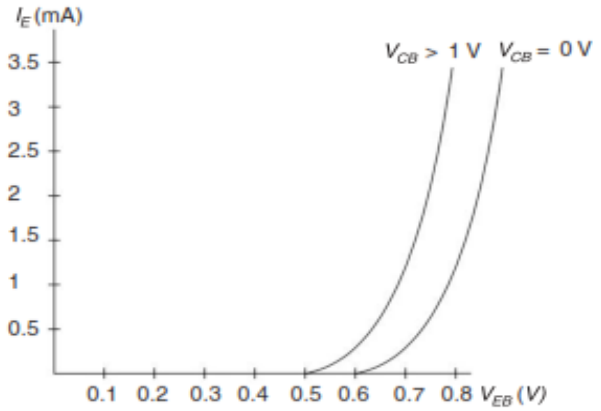
CB Configuration:



Circuit to determine CB static characteristics

Input Characteristics To determine the input characteristics, the collector-base voltage V_{CB} is kept constant at zero volt and the emitter current I_E is increased from zero in suitable equal steps by increasing V_{EB}. This is repeated for higher fixed values of V_{CB}. A curve is drawn between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}. The input characteristics thus obtained are shown in Fig.

When V_{CB} is equal to zero and the emitter-base junction is forward biased as shown in the characteristics, the junction behaves as a forward-biased diode so that emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB}. When V_{CB} is increased keeping V_{EB} constant, the width of the base region will decrease. This effect results in an increase of I_E. Therefore, the curves shift towards the left as V_{CB} is increased.



CB input characteristics

Transistor Parameters :

The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common-base *hybrid parameters* or *h-parameters*.

- **Input Impedance (h_{ib})** It is defined as the ratio of the change in (input) emitter voltage to the change in (input) emitter current with the (output) collector voltage V_{CB} kept constant. Therefore,

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, V_{CB} \text{ constant}$$

It is the slope of CB input characteristics I_E versus V_{EB} The typical value of h_{ib} ranges from 20 Ω to 50 Ω.

- **Output Admittance (h_{ob})** It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) emitter current I_E kept constant. Therefore,

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, I_E \text{ constant}$$

It is the slope of CB output characteristics I_C versus V_{CB}. The typical value of this parameter is of the order of 0.1 to 10 μ mhos.

- **Forward Current Gain (h_{fb})** It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage V_{CB} constant. Hence,

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, V_{CB} \text{ constant}$$

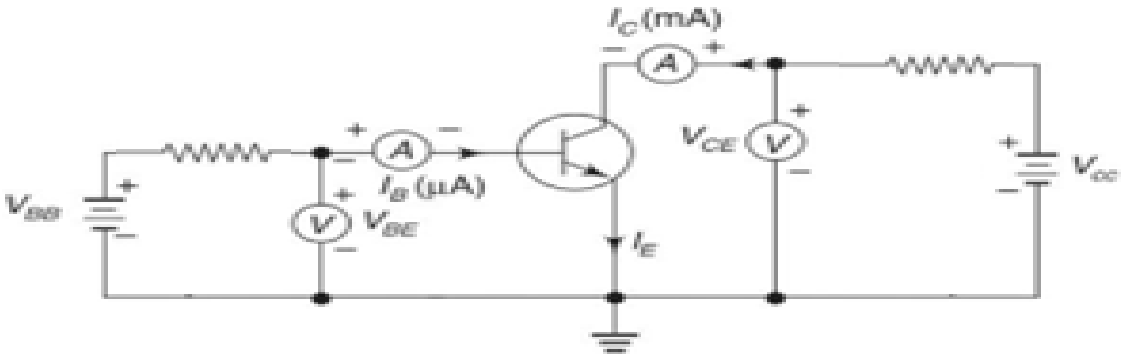
It is the slope of I_C versus I_E curve. Its typical value varies from 0.9 to 1.0.

- **Reverse Voltage Gain (h_{rb})** It is defined as the ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current, I_E. Hence,

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, I_E \text{ constant}$$

It is the slope of V_{EB} versus V_{CB} curve. Its typical value is of the order of 10^{-5} to 10^{-4}.

Common Emitter configuration:

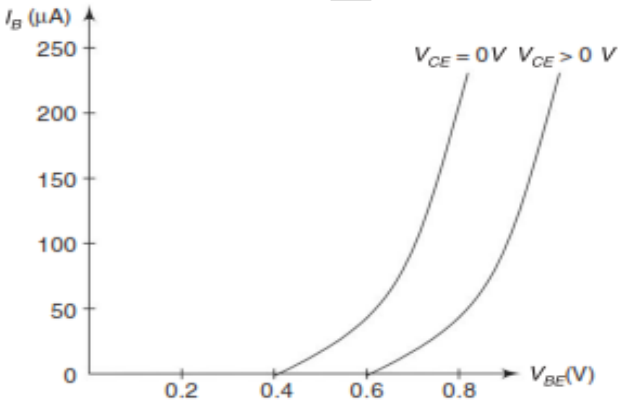


Circuit to determine CE static characteristics

Input Characteristics :

The value of V_{BE} is noted for each setting of I_B. This procedure is repeated for higher fixed values of V_{CE}, and the curves of I_B V_s. V_{BE} are drawn. The input characteristics thus obtained are shown in Fig.

When $V_{CE} = 0$, the emitter-base junction is forward biased and the junction behaves as a forward biased diode. Hence, the input characteristic for $V_{CE} = 0$ is similar to that of a forward-biased diode. When V_{CE} is increased, the width of the depletion region at the reverse-biased collector-base junction will increase. Hence, the effective width of the base will decrease. This effect causes a decrease in the base current I_B. Hence, to get the same value of I_B as that for $V_{CE} = 0$, V_{BE} should be increased. Therefore, the curve shifts to the right as V_{CE} increases.

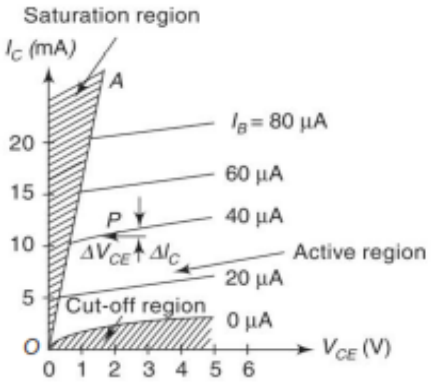


CE input characteristics

Output Characteristics To determine the output characteristics, the base current I_B is kept constant at a suitable value by adjusting the base-emitter voltage, V_{BE}. The magnitude of the collector-emitter voltage V_{CE} is increased in suitable equal steps from zero and the collector current I_C is noted for each setting V_{CE}. Now, the curves of I_C versus V_{CE} are plotted for different constant values of I_B. The output characteristics thus obtained are shown in Fig. 4.12.

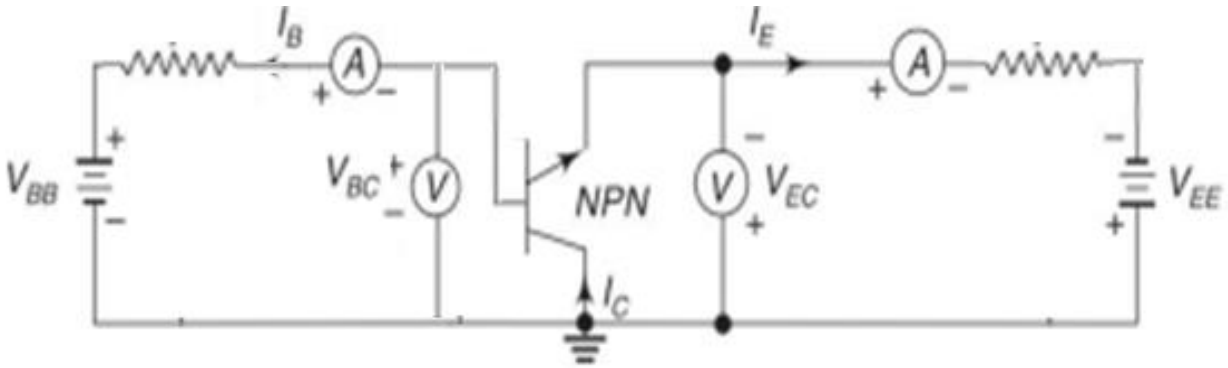
From Eqs. (4.11) and (4.12), we have

$$\beta = \frac{\alpha}{1-\alpha} \quad \text{and} \quad I_C = (1+\beta)\, I_{CBO} + \beta I_B$$



CE output characteristics

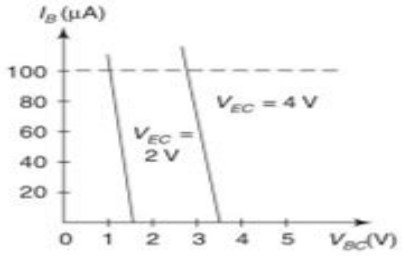
Common Collector configuration:



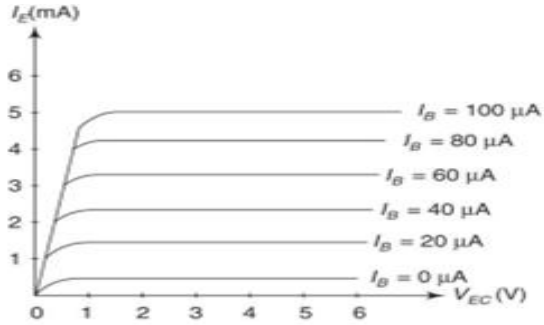
Circuit to determine CC static characteristics

Input Characteristics To determine the input characteristics, V_{EC} is kept at a suitable fixed value. The base-collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for different fixed values of V_{EC}. Plots of V_{BC} versus I_B for different values of V_{EC} shown in Fig are the input characteristics.

Output Characteristics To determine the output characteristics, the base current, I_B, is kept constant at a suitable value by adjusting the base-collector voltage, V_{BC}. The magnitude of the emitter-collector voltage, V_{EC}, is increased in suitable equal steps from zero and the emitter current, I_E, is noted for each setting V_{EC}. Now, the curves of I_E versus V_{EC} are plotted for different constant values of I_B. The output characteristics thus obtained are shown in Fig. . These output characteristics are the same as those of the common emitter configuration.



CC input characteristics



CC output characteristics

CLASS-12

Comparison of Different Configurations:

Property	CB	CE	CC
Input resistance	Low (about 100 Ω)	Moderate (about 750 Ω)	High (about 750 kΩ)
Output resistance	High (about 450 kΩ)	Moderate (about 45 kΩ)	Low (about 25 Ω)
Current gain	1	High	High
Voltage gain	About 150	About 500	Less than 1
Phase shift between input and output voltages	0 or 360°	180°	0 or 360°
Applications	for high frequency circuits	for audio frequency circuits	for impedance matching

Early Effect :

Early Effect or Base Width Modulation As the collector voltage V_{CC} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base width on collector-to-base voltage is known as the *Early effect*. This decrease in effective base width has three consequences:

(i) There is less chance for recombination within the base region. Hence, α increases with increasing $|V_{CB}|$.

(ii) The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.

(iii) For extremely large voltages, the effective base width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the *punch-through*.

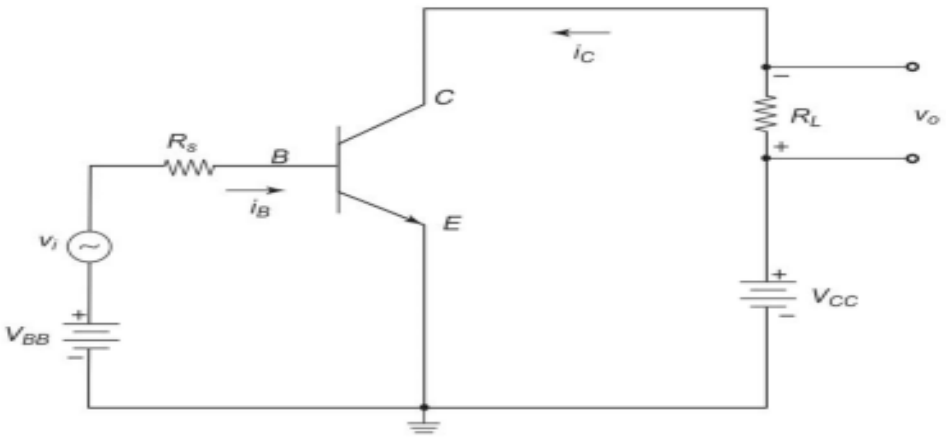
For higher values of V_{CB}, due to Early effect, the value of α increases. For example, α changes, say from 0.98 to 0.985. Hence, there is a very small positive slope in the CB output characteristics and, hence, the output resistance is not zero.

Punch through/ reach through:

The Early effect widens the collector-junction depletion region with increased collector voltage. As VEB increases, the transition region extends into the base, affecting output characteristics and causing a positive slope in the IE vs. VEB curve. Input impedance is also influenced by VEB, and increasing base doping reduces emitter efficiency by raising the punch-through voltage..

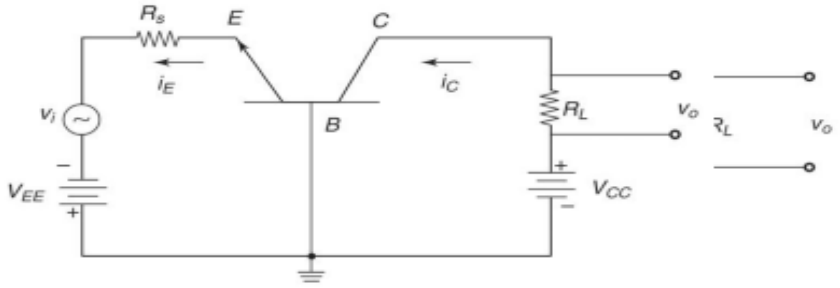
Transistor as an amplifier:

A CE amplifier circuit uses an NPN transistor in a common-emitter configuration. The VBB supply forward-biases the emitter-base junction, while VCC reverse-biases the collector-base junction, ensuring active region operation.



CE transistor as an amplifier

CB Transistor as an Amplifier:



CB transistor as an amplifier

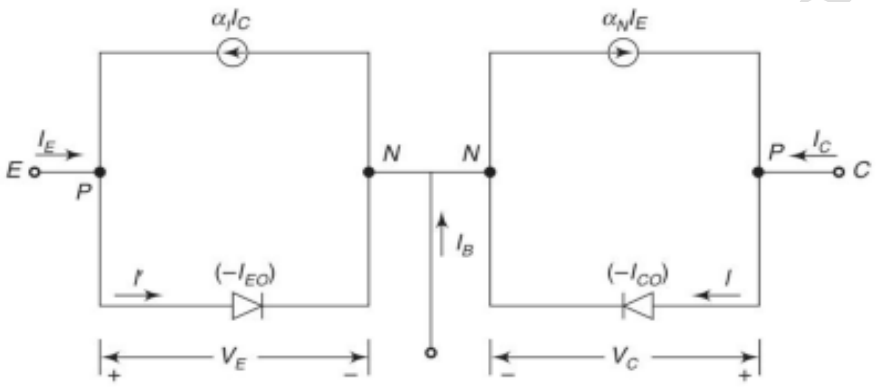
CLASS-13

Ebers-Moll model of a transistor:

The general expression for collector current I_C of a transistor for any voltage across the collector junction V_C and emitter current I_E is

$$I_C = -\alpha_N I_E - I_{CO}\left(e^{\frac{V_C}{V_T}} - 1\right)$$

where α_N is the current gain in *normal* operation and I_{CO} is the collector-junction reverse saturation current. In inverted mode of operation, the above equation can be written as



Ebers–Moll model for a PNP transistor

CLASS-14

Large Signal, DC and Small Signal CE Values of Current Gain :

The dc current gain of the transistor is given by

$$\beta_{dc} \equiv h_{FE} \equiv \frac{I_C}{I_B}$$

Based on this h_{FE} value, we can determine whether the transistor is in saturation or not. For any transistor, in general, I_B is large compared to I_{CBO}. Under this condition, the value of $h_{FE} \approx \beta$.

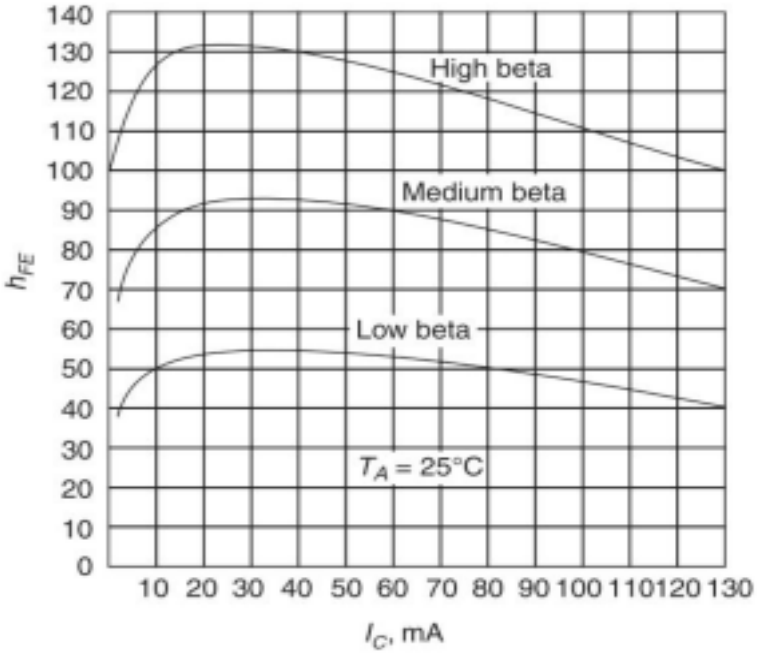
The small-signal CE forward short-circuit gain β' is defined as the ratio of a collector-current increment ΔI_C for a small base-current change ΔI_B, at a fixed collector-to-emitter voltage V_{CE}.

i.e., $$\beta' \equiv \left.\frac{\partial I_C}{\partial I_B}\right|_{V_{CE}}$$

If β is independent of currents then $\beta' = \beta \approx h_{FE}$. However, β is a function of current, then $\beta' = \beta + (I_{CBO} + I_B)\frac{\partial \beta}{\partial I_B}$. By using $\beta' = h_{fe}$ and $\beta \approx h_{FE}$. Therefore, the above equation becomes

$$h_{fe} = \frac{h_{FE}}{1 - (I_{CBO} + I_B)\frac{\partial h_{FE}}{\partial I_C}}$$

In Fig. 4.17, the h_{FE} versus I_C shows a maximum and, hence, $h_{fe} > h_{FE}$ for smaller currents, and $h_{fe} < h_{FE}$ for larger currents. Therefore, the above equation is valid only for the active region.

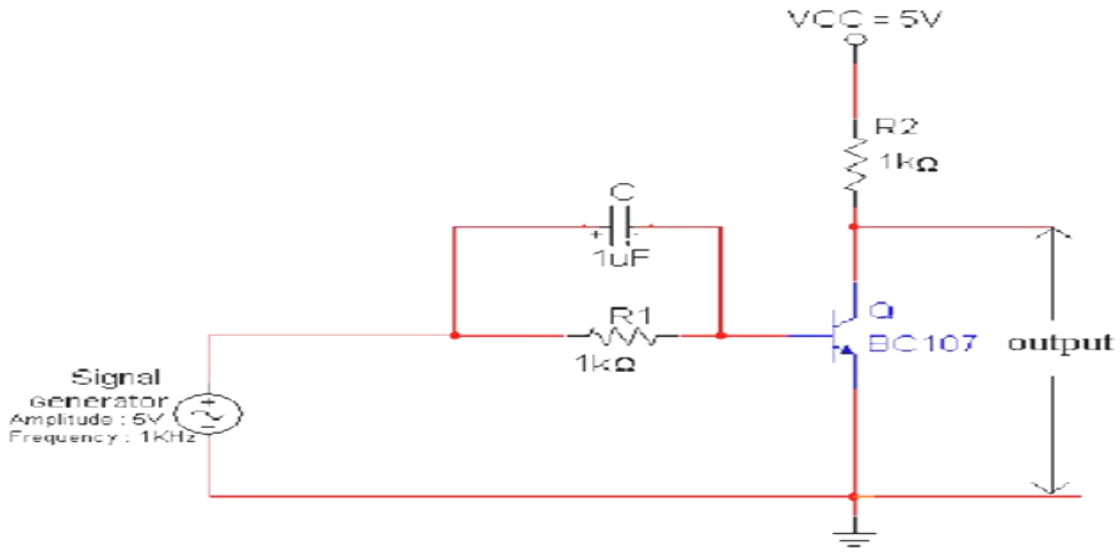


Characteristic curves of dc current gain h_{FE} (at $V_{CE} = -0.25$ V) versus collector current for low, medium, and high beta values

CLASS-15

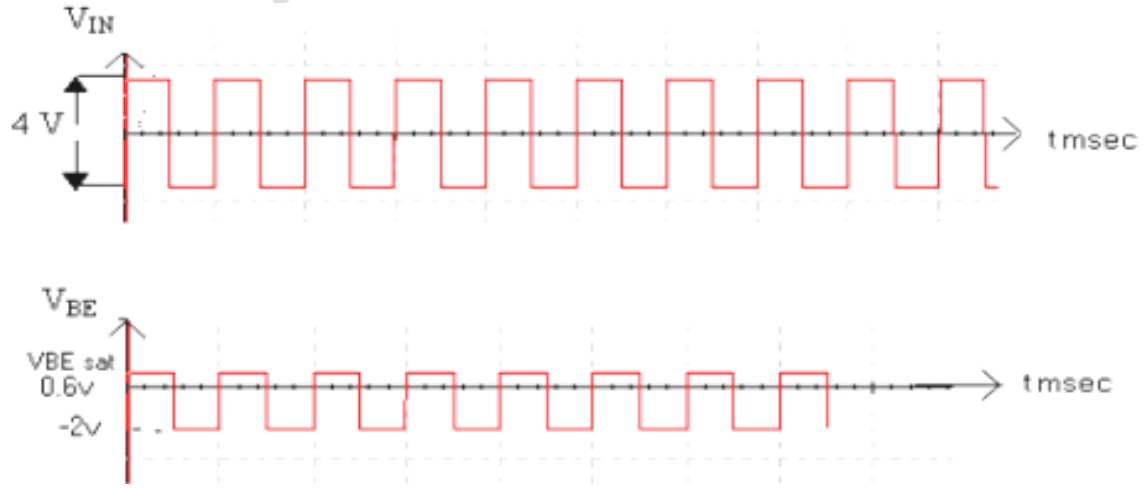
Transistor as a Switch:

A transistor used as a switch operates in two states: cut-off (OFF) and saturation (ON). In the cut-off region, no base current flows (IB = 0), keeping the base-emitter junction non-conductive (VBE < 0.7V for silicon), resulting in zero collector current (IC ≈ 0) and an open switch behavior. In the saturation region, a sufficient base current forward biases the base-emitter junction (VBE ≈ 0.7V), reducing the collector-emitter voltage (VCE ≈ 0.1V–0.3V) and allowing maximum current flow, making the transistor act as a closed switch.



Circuit diagram of transistor working as a switch

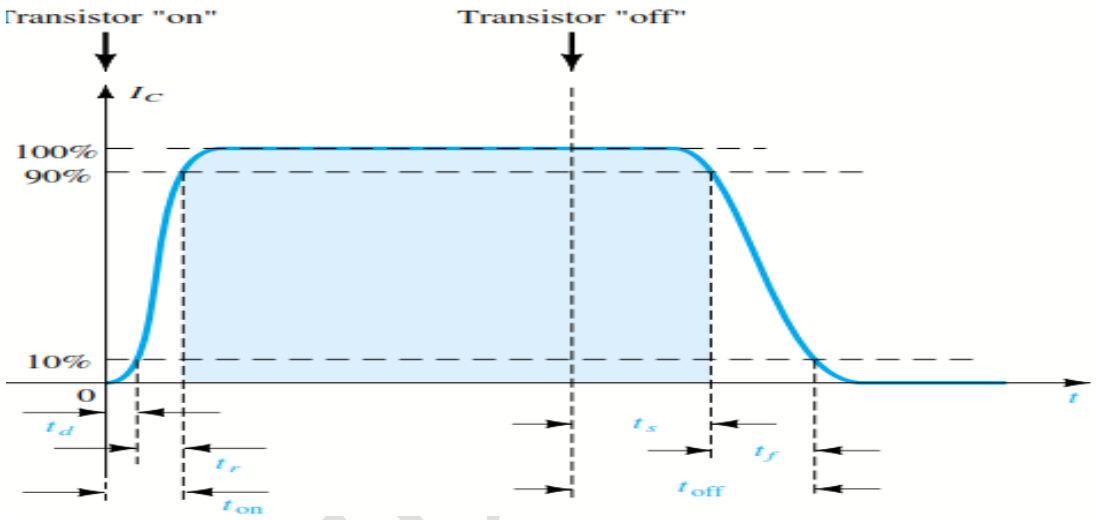
Transistors in digital and switching circuits alternate between LOW (0V) and HIGH (+5V) states. They operate in cutoff (OFF) with both junctions reverse biased, allowing only negligible reverse current, and in saturation (ON) with both junctions forward biased, resulting in small VCE(sat) and VBE(sat).



CLASS-16

Transistor Switching Times :

Transistor switching time is crucial in high-frequency applications and consists of delay time (td), rise time (tr), storage time (ts), and fall time (tf). Delay time is when the input signal is applied until the collector current starts changing. Rise time is when the collector current increases from 10% to 90%. Storage time is when the base drive is removed until the collector current starts decreasing. Fall time is when the collector current drops from 90% to 10%. The total switching time is the sum of td and tr for turning ON (ton) and ts and tf for turning OFF (toff).



Defining the time intervals of a pulse waveform

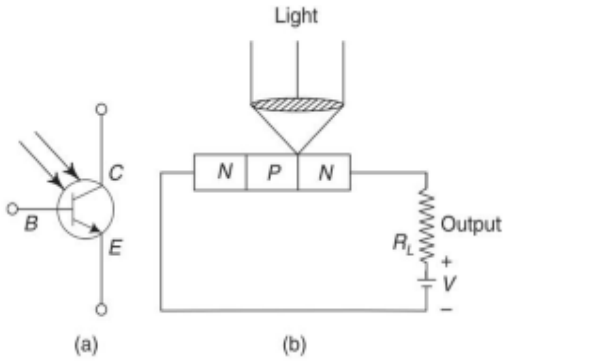
CLASS-17

Maximum Voltage Rating:

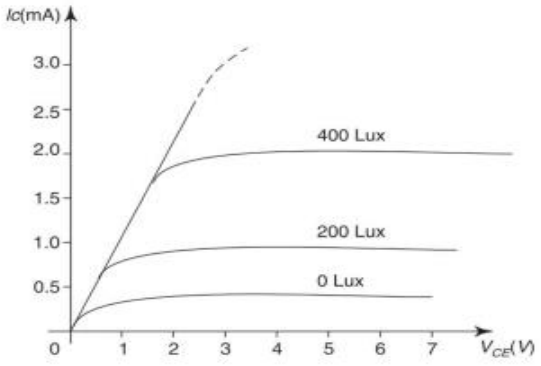
The maximum voltage rating of a transistor is the highest voltage it can handle without damage. Exceeding this can cause breakdown effects like avalanche breakdown or punch-through. Different voltage ratings apply to various transistor terminals and must be adhered to for safe operation.

Photo Transistor:

A phototransistor is a highly sensitive light detector that integrates a photodiode and a transistor amplifier. Unlike a PN photodiode, its output current is stronger and can directly control circuits. Typically configured as an NPN transistor in a common-emitter (CE) setup with an open base, it uses a lens to focus light on the base-collector junction. The light-generated current at this junction acts as the base current, enabling a larger collector-emitter current flow. Only the emitter and collector terminals are usually used.



NPN phototransistor: (a) Symbol (b) Biasing arrangement

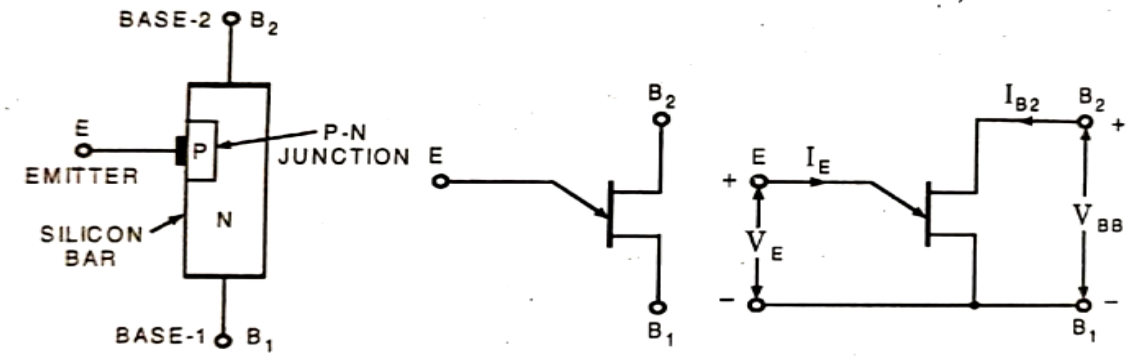


Characteristics of a phototransistor

CLASS-18

UJT- Uni Junction Transistor :

Unijunction transistor (abbreviated as UJT), also called the *double-base diode*, is a 2 layer, 3 terminal solid-state (silicon) switching device. The device has a unique characteristic that when it is triggered, its emitter current increases regeneratively (due to negative resistance characteristic) until it is restricted by emitter power supply. The low cost per unit, combined with its unique characteristics, have warranted its use in a wide variety of applications. A few include oscillators, pulse generators, sawtooth generators, trigger circuits, phase control, timing circuits, and voltage- or current-regulated supplies. The device is, in general, a low-power absorbing device under normal operating conditions and provides tremendous aid in the continual effort to design relatively efficient systems.



(a) Basic Structure *(b) Schematic Symbol* *(c) Basic Arrangement*

The single P-N junction accounts for the terminology *unijunction*. The silicon bar, at its ends, has two ohmic contacts designated as base-1 (B_1) and base-2 (B_2), as shown and the P-type region is termed the emitter (E). The emitter junction is usually located closer to base-2 (B_2) than base-1 (B_1) so that the device is not symmetrical, because symmetrical unit does not provide optimum electrical characteristics for most of the applications.

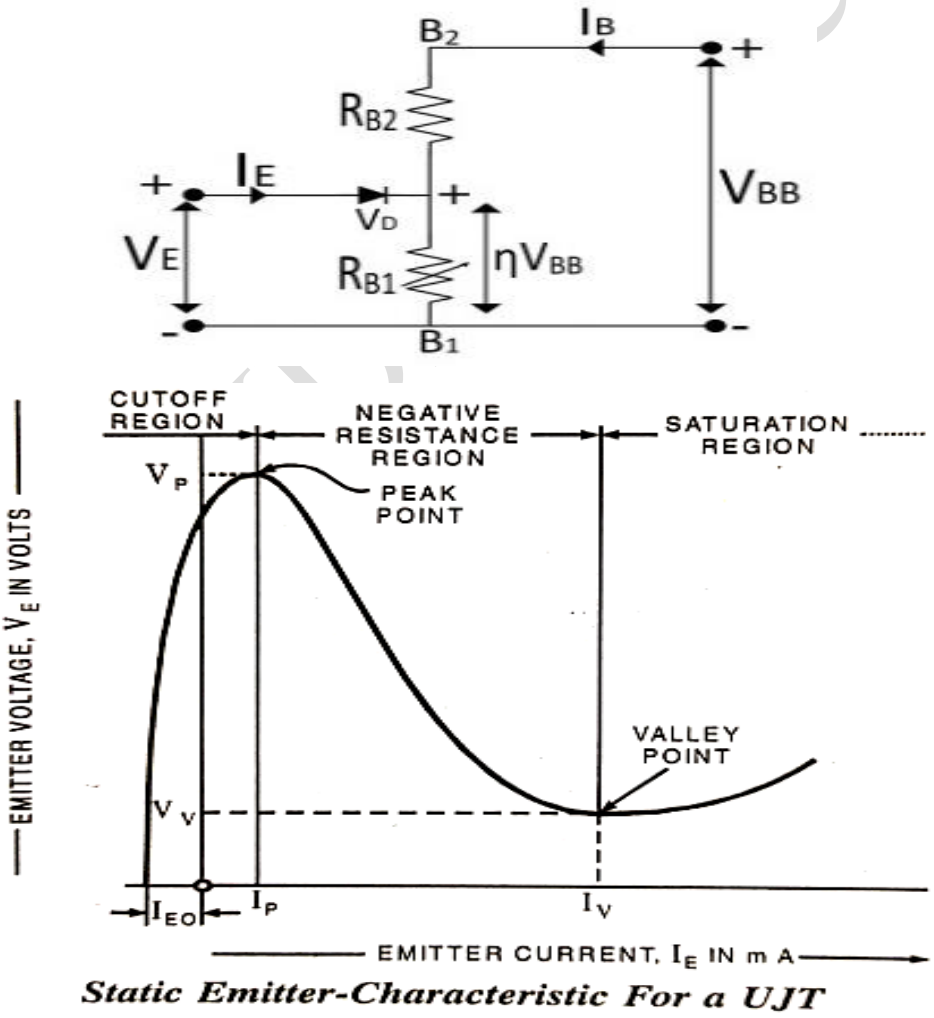
The emitter leg is drawn at an angle to the vertical line representing the N-type material slab and the arrowhead points in the direction of *conventional current* when the device is forward biased, active or in the conducting state. The basic arrangement for the UJT

Operation of UJT

With Emitter Open :

When voltage **VBB** is applied with an open emitter, a potential gradient forms along the **n-type silicon bar**. Since the **emitter** is near **base B2**, most of **VBB** appears between the **emitter and base B1**, reverse biasing the **pn-junction** and cutting off the **emitter current (IE)**, except for a small leakage current from **B2 to emitter** due to **minority carriers**. This is the **OFF state**.

When the **emitter is at a positive potential**, the **pn-junction** stays reverse biased until the emitter voltage exceeds **V1**. Beyond this, the junction becomes **forward biased**, injecting **holes** into the **n-type bar**. These holes move from **emitter to B1**, reducing resistance and increasing **IE**. As more holes are supplied, the device reaches **saturation**, where **IE** is limited by the **power supply**, switching the device **ON**.



Static Emitter-Characteristic For a UJT

Advantages of UJT

Low cost

Excellent characteristics

Low power absorbing device under normal operating conditions

Applications of UJT

Oscillators

Trigger Circuits

Saw tooth generator

Bi-stable networks

Pulse and voltage sensing circuits

UJT relaxation oscillators

Over voltage detectors

UNIT- 3: Field Effect Transistor (FET) Characteristics

S.No	Topic Name
1.	The Junction Field-Effect Transistor (JFET)-Types,
2.	Construction and Operation, the Pinch-Off Voltage,
3.	JFET Characteristics,
4.	JFET Parameters,
5.	JFET Equivalent Circuits,
6.	JFET Applications,
7.	Comparison Between BJT and JFET,
8.	Metal-Oxide-Semiconductor FET (MOSFET)- Types,
9.	Construction, Operation and Characteristics,
10.	Comparison Between JFET and MOSFET,
11.	Introduction to MOS, CMOS and Bi-CMOS Logics,
12.	NMOS, CMOS and Bi-CMOS Inverter Circuits.

CLASS-19

FET types:

FETs are classified into JFET (N-Channel and P-Channel) and MOSFET based on construction. A typical FET has an N-type silicon bar with source (S), drain (D), and gate (G).

- **Source (S):** Connected to the negative terminal; electrons enter.
- **Drain (D):** Connected to the positive terminal; electrons exit.
- **Gate (G):** P-type silicon forms the PN junctions with the N-type bar.
- **Channel:** Region between depletion layers where majority carriers flow.

Operation: Current flows through the channel, controlled by the gate voltage. FETs offer high input impedance, low power consumption, and regulate current using an electric field.

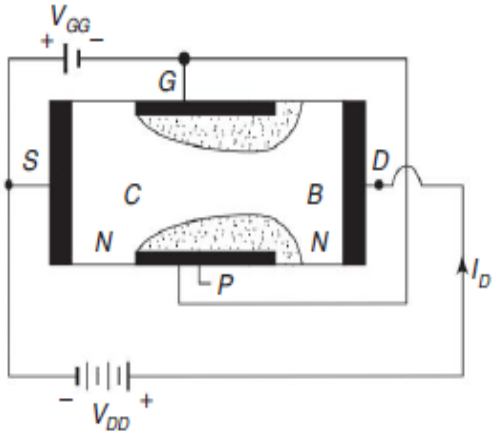
the conventional current I_D flows from drain to source. The magnitude of the current will depend upon the following factors:

1. The number of majority carriers (electrons) available in the channel, i.e., the conductivity of the channel.
2. The length L of the channel.
3. The cross-sectional area A of the channel at B.
4. The magnitude of the applied voltage V_{DS}. Thus, the channel acts as a resistor of resistance R given by

$$R = \frac{\rho L}{A} \qquad (4.31)$$

$$I_D = \frac{V_{DS}}{R} = \frac{A V_{DS}}{\rho L} \qquad (4.32)$$

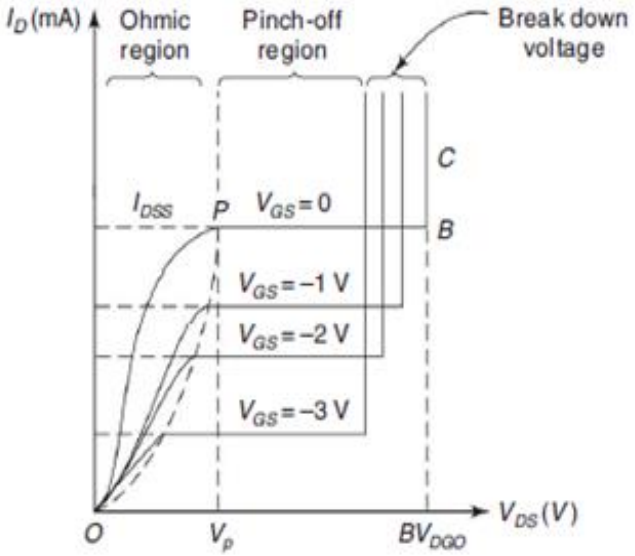
where ρ is the resistivity of the channel. Because of the resistance of the channel and the applied voltage V_{DS}, there is a gradual increase of positive potential along the channel from source to drain. Thus, the reverse voltage across the PN junctions increases and hence the thickness of the depletion regions also increases. Therefore, the channel is wedge-shaped as shown in Fig.



JFET under applied bias

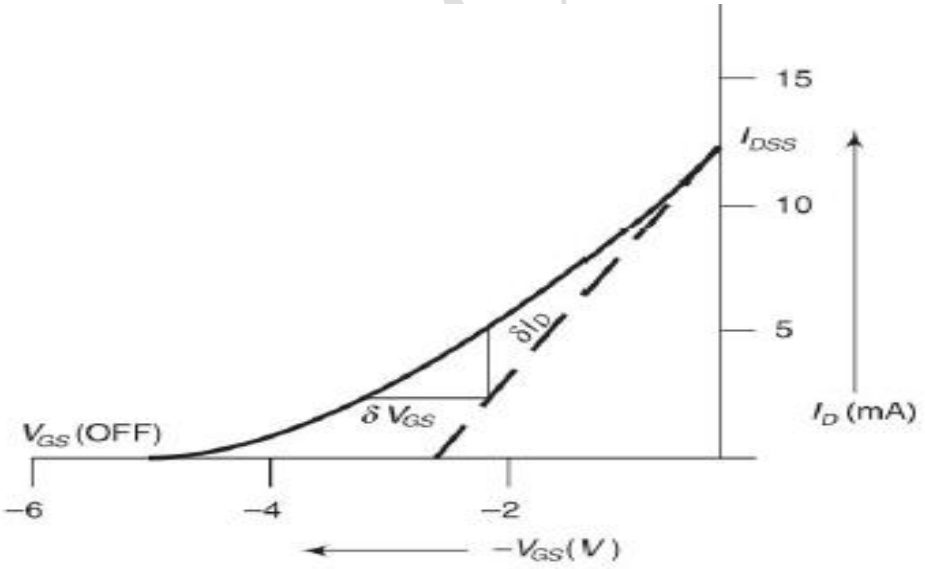
(i) As V_{DS} is increased from zero, I_D increases along OP, and the rate of increase of I_D with V_{DS} decreases as shown in Fig. 4.26. The region from $V_{DS} = 0$ V to $V_{DS} = V_P$ is called the ohmic region. In the ohmic region, the drain-to-source resistance $\frac{V_{DS}}{I_D}$ is related to the gate voltage V_{GS}, in an almost linear manner. This is useful as a Voltage Variable Resistor (VVR) or Voltage Dependent Resistor (VDR).

(ii) When $V_{DS} = V_P$, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off or saturation region increases. Hence, there is no further increase of I_D.



Drain characteristics

(iii) At a certain voltage corresponding to the point B, I_D suddenly increases. This effect is due to the avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and the drain. The drain voltage at which the breakdown occurs is denoted by BV_{DGO}. The variation of I_D with V_{DS} when $V_{GS} = 0$ is shown in Fig. by the curve $OPBC$.



Transfer characteristics of JFET

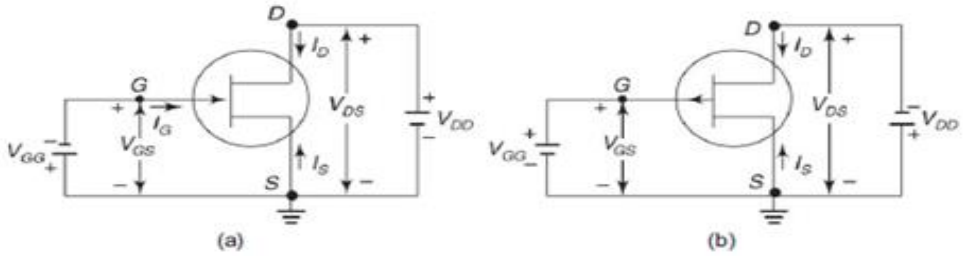
- **When V_{GS} is Negative and V_{DS} is Increased** When the gate is maintained at a negative voltage less than the negative cut-off voltage, the reverse voltage across the junction is further increased. Hence, for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for $V_{GS} = 0$, but the values of V_P and BV_{DGO} are lower, as shown in

From the curves, it is seen that above the pinch-off voltage, at a constant value of V_{DS}, I_D increases with an increase of V_{GS}. Hence, a JFET is suitable for use as a voltage amplifier, similar to a transistor amplifier.

It can be seen from the curve that for voltage $V_{DS} = V_P$, the drain current is not reduced to zero. If the drain current is to be reduced to zero, then the ohmic voltage drop along the channel should also be reduced to zero. Further, the reverse biasing to the gate-source PN junction essential for pinching off the channel would also be absent.

The drain current I_D is controlled by the electric field that extends into the channel due to reverse-biased voltage applied to the gate; hence, this device has been given the name *Field Effect Transistor*.

In a bar of P-type semiconductor, the gate is formed due to N-type semiconductor. The working of the P-channel JFET will be similar to that of N-channel JFET with proper alterations in the biasing circuits; in this case, holes will be the current carriers instead of electrons. The circuit symbols for N-channel and P-channel JFETs are shown in Fig. It should be noted that the direction of the arrow points in the direction of conventional current which would flow into the gate if the PN junction was forward biased.



Circuit symbols for (a) N-Channel JFET and (b) P-channel JFET

CLASS-20

Parameters (JFET):

In a JFET, the drain current I_D depends upon the drain voltage V_{DS} and the gate voltage V_{GS}. Any one of these variables may be fixed and the relation between the other two are determined. These relations are determined by the three parameters which are defined below.

Mutual Conductance or Transconductance, g_m It is the slope of the transfer characteristic curves, and is defined by

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} = \frac{\Delta I_D}{\Delta V_{GS}}, V_{DS} \text{ held constant}$$

It is the ratio of a small change in the drain current to the corresponding small change in the gate voltage at a constant drain voltage. The change in I_D and V_{GS} should be taken on the straight part of the transfer characteristics. It has the unit of conductance in mho.

Drain Resistance, r_d It is the reciprocal of the slope of the drain characteristics and is defined by

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D}, V_{GS} \text{ held constant}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in the drain current at a constant gate voltage. It has the unit of resistance in ohms.

The drain resistance at $V_{GS} = 0$ V, i.e., when the depletion regions of the channel are absent, is called as *drain-source ON resistance*, represented as R_{DS} or $R_{DS(ON)}$.

The reciprocal of r_d is called the drain conductance. It is denoted by g_d or g_{ds}.

Amplification Factor, μ It is defined by

$$\mu = \left(\frac{\partial V_{DS}}{\partial V_{GS}}\right) I_D = -\frac{\Delta V_{DS}}{\Delta V_{GS}}, I_D \text{ held constant}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in the gate voltage at a constant drain current. Here, the negative sign shows that when V_{GS} is increased, V_{DS} must be decreased for I_D to remain constant.

Expression for saturation drain current:

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

CLASS-21

ApplicationsofJFET :

- Used as buffers in measuring instruments and receivers (high input, low output impedance).
- Found in RF amplifiers for low noise in FM tuners and communication devices.
- Ideal for cascade amplifiers in test equipment due to low input capacitance.
- Act as voltage-variable resistors in operational amplifiers and tone controls.
- Used in mixer circuits in FM/TV receivers for low intermodulation distortion.
- Help in oscillator circuits with low frequency drift.

.

Comparison of JFET and BJT

FET vs. BJT:

FETs use only majority carriers (unipolar), while BJTs use both majority and minority carriers. FETs are less noisy, have high input impedance, and work well as buffer amplifiers, unlike BJTs. FETs are voltage-controlled, while BJTs are current-controlled. FETs are smaller, easier to fabricate, and radiation-resistant. They handle temperature changes better and have higher switching speeds, while BJTs are prone to thermal breakdown and slower switching.

FET amplifiers have low gain-bandwidth and higher signal distortion, while BJTs are cheaper to produce.

CLASS-22

JFET Equivalent Circuits :

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the FET transistor in the ac domain can be constructed. The control of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 9.8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

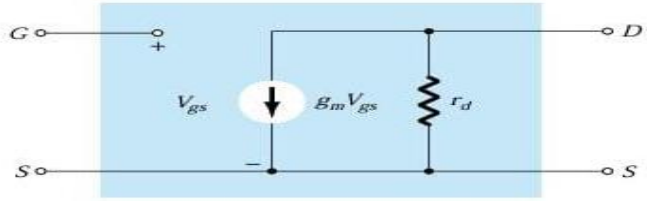


Figure 9.8 FET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source. Note that the gate to source voltage is now represented by V_{gs} (lower-case subscripts) to distinguish it from dc levels. In addition, take note of the fact that the source is common to both input and output circuits while the gate and drain terminals are only in "touch" through the controlled current source $g_m V_{gs}$.

In situations where r_d is ignored (assumed sufficiently large to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply a current source whose magnitude is controlled by the signal V_{gs} and parameter g_m—clearly a voltage-controlled device.

MOSFET-types:

MOSFET (IGFET):

MOSFET, also called IGFET, has two types: Enhancement MOSFET and Depletion MOSFET.

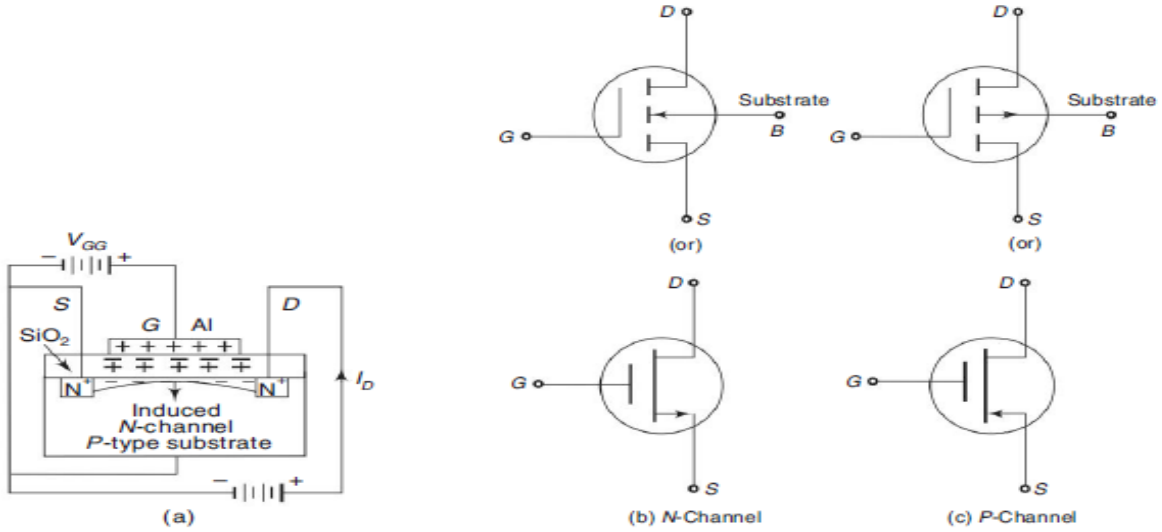
Principle: A transverse electric field across an insulator controls the thickness and resistance of the conducting channel.

- Depletion MOSFET: The electric field reduces majority carriers, decreasing conduction.
- Enhancement MOSFET: The electric field increases majority carriers, improving conduction.

CLASS-23

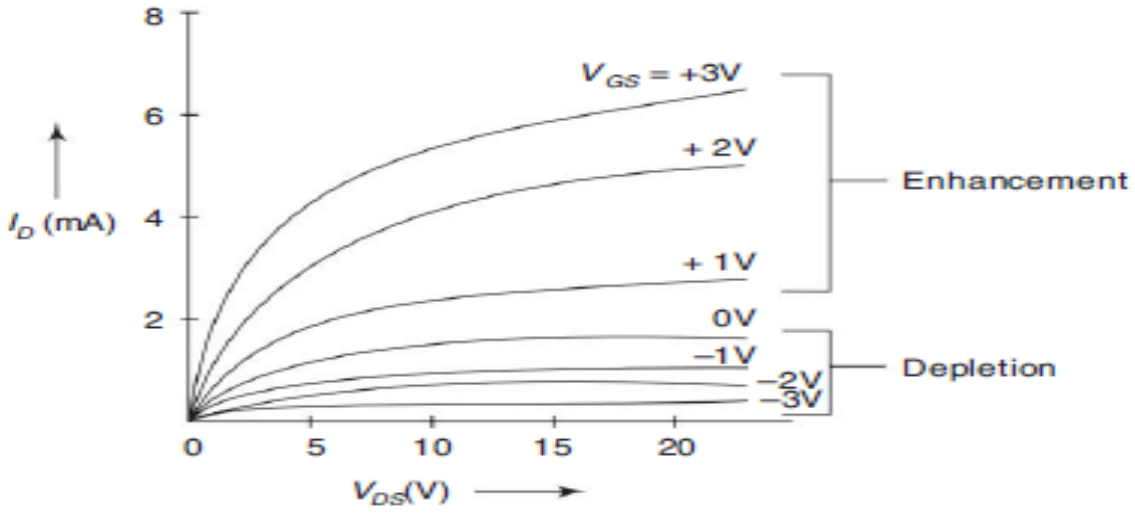
MOSFET -Construction, operation and characteristics:

Construction:



(a) N-channel enhancement MOSFET (b) and (c) Circuit symbols for enhancement MOSFET

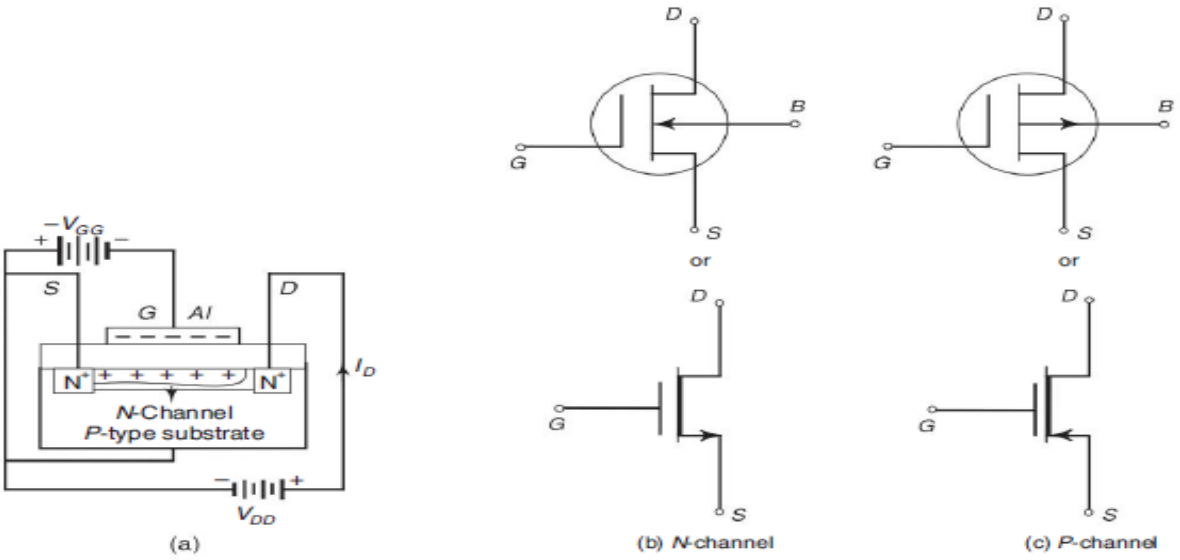
CHARACTERISTICS OF MOSFET:



Volt-ampere characteristics of MOSFET

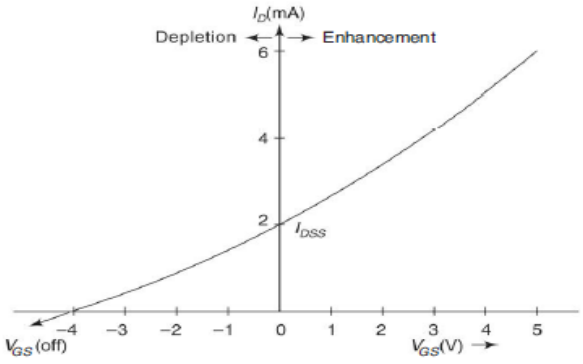
Depletion MOSFET:

In an N-channel depletion MOSFET, with VGS = 0 and a positive drain potential, electrons flow from source to drain, creating ID. A negative gate voltage depletes electrons, forming a depletion region. As VDS increases, ID rises, stabilizing at pinch-off voltage. Beyond this, ID remains constant. Negative VGS reduces conductivity, lowering ID.



(a) N-channel depletion MOSFET, (b) and (c) Circuit symbols for depletion MOSFETs

The curve of I_D versus V_{GS} for constant V_{DS} is called the transfer characteristics of the MOSFET and is shown in Fig.



Transfer characteristics of MOSFET

CLASS-24

Comparison between JFET and MOSFET:

MOSFET vs. JFET:

In **MOSFETs**, a **transverse electric field** across an **insulating layer** controls conductivity, while in **JFETs**, it is controlled by a **reverse-biased PN junction**.

MOSFETs have **higher input resistance** (10^{10}–10^{15} Ω) with **lower gate leakage current** (10^{-12} A) than **JFETs** (10^{8} Ω, 10^{-9} A). **JFETs** have **flatter output characteristics** and **higher drain resistance** (0.1–1 MΩ) than **MOSFETs** (1–50 kΩ).

JFETs work only in **depletion mode**, while **depletion MOSFETs** operate in **both modes**. **MOSFETs** are **easier to fabricate** but **prone to voltage damage**. They have **zero offset voltage**, allowing **source-drain interchange**, useful in **analog switching**.

CMOS circuits offer **low power use**, making **MOSFETs ideal for portable devices** and **VLSI circuits**, unlike JFETs.

CLASS-25

Introduction to MOS, CMOS and Bi-CMOS Logics :

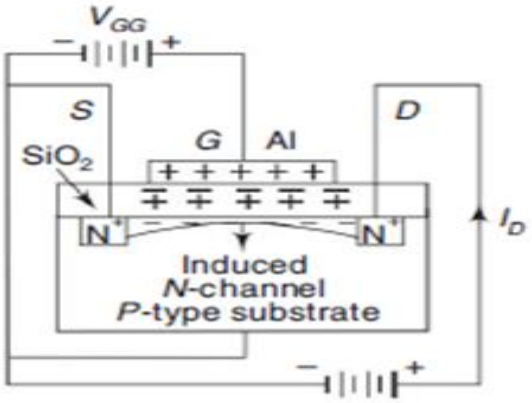
MOS (Metal-Oxide-Semiconductor) Logic

MOS Logic utilizes MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) as the fundamental building blocks in digital circuits.

Types of MOSFETs:

NMOS (n-channel MOSFET) and PMOS (p-channel MOSFET).

NMOS Logic:



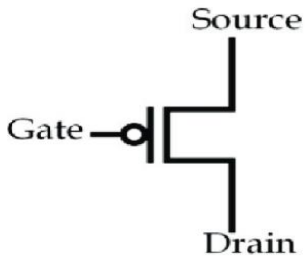
Only NMOS transistors are used. They are fast but consume power in standby mode due to current flow through the pull-up resistor.

S. No	V_{in} (V_{GS})	State of the NMOS
1.	0 or Low	OFF
2.	1 or High	ON

PMOS Logic:

Only PMOS transistors are used. They are slower than NMOS and used less frequently due to higher threshold voltages and larger sizes.

S. No	V_{in} (V_{GS})	State of the PMOS
1.	0 or Low	ON
2.	1 or High	OFF



Comparison between NMOS and PMOS

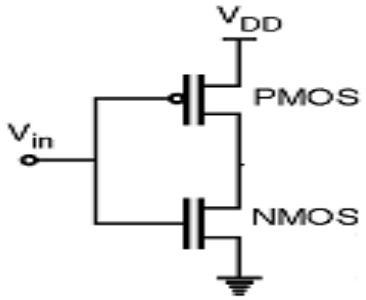
P-Channel is much easier and cheaper to produce than the N-Channel device.

S.NO	NMOS	PMOS
1.	Uses n-type material for the channel; conducts when a positive voltage is applied to the gate.	Uses p-type material for the channel; conducts when a negative voltage is applied to the gate.
2.	Higher electron mobility results in faster operation.	Lower hole mobility leads to slower operation compared to NMOS.
3.	Consumes more power during switching due to higher current flow.	Consumes less power during switching but is less efficient overall.
4.	Requires a positive threshold voltage to turn ON.	Requires a negative threshold voltage to turn ON.
5.	Preferred for high-speed and high-performance circuits due to faster electron mobility.	Often used in low-power applications and as pull-up devices in CMOS technology.

CLASS-26

CMOS (Complementary Metal-Oxide-Semiconductor) Logic

CMOS uses both NMOS and PMOS transistors in a complementary structure.



Characteristics:

Low static power consumption: no current flows when output is in a steady state.

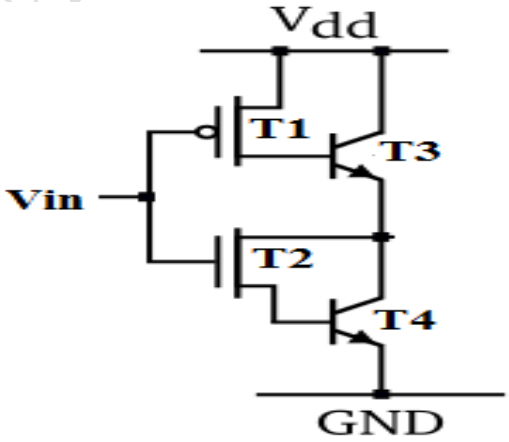
High noise immunity and excellent speed-power product.

Utilized widely in modern IC design due to its efficiency and scalability.

S. No	V_{in} (V_{GS})	PMOS	NMOS
1.	0 or Low	ON	OFF
2.	1 or High	OFF	ON

Bi-CMOS (Bipolar-CMOS) Logic

Bi-CMOS combines the high-speed characteristics of Bipolar Junction Transistors (BJTs) with the low-power, high-density characteristics of CMOS.



S. No	V_{in} (V_{GS})	T1	T2	T3	T4
1.	0 or Low	ON	OFF	ON	OFF
2.	1 or High	OFF	ON	OFF	ON

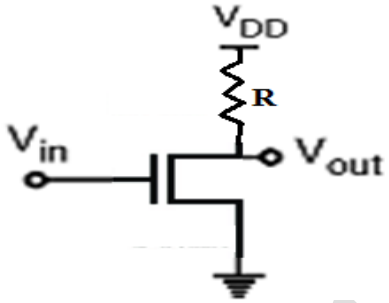
CLASS-27

NMOS, CMOS and Bi-CMOS Inverter Circuits :

NMOS Inverter Circuit

Configuration:

Consists of an NMOS transistor with a resistor as a pull-up.



The NMOS transistor acts as a switch: it is ON when the input is high (logic 1) and OFF when the input is low (logic 0).

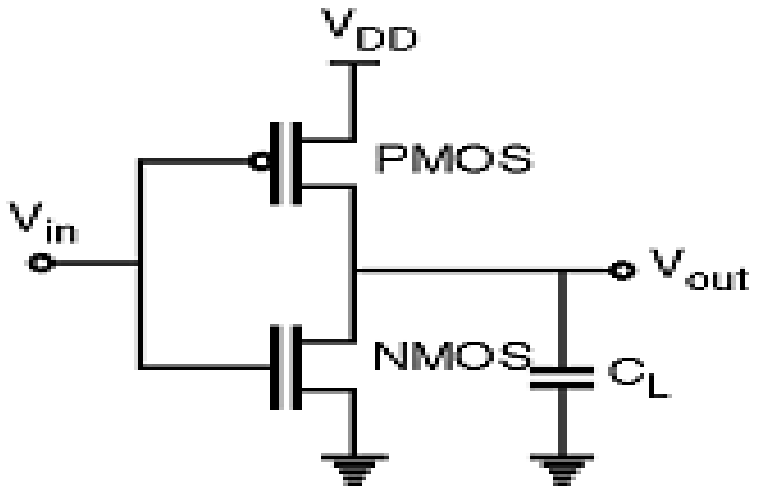
S. No	V_{in} (V_{GS})	State of the NMOS	output is pulled
1.	0 or Low	OFF	High
2.	1 or High	ON	Low

CLASS-28

CMOS Inverter Circuit

CMOS Configuration:

A CMOS inverter has a complementary NMOS and PMOS pair. The NMOS drain (D) and gate (G) are connected, VDD is at the PMOS source, and GND at the NMOS source. Vin goes to both gate terminals, while Vout is at the drain terminals of both transistors.



S. No	V_{in} (V_{GS})	PMOS	NMOS	V_{OUT}
1.	0 or Low	ON	OFF	1
2.	1 or High	OFF	ON	0

CMOS Operation:

NMOS is connected to GND, PMOS to VDD.

- Input Low → PMOS ON, NMOS OFF, Vout High
- Input High → NMOS ON, PMOS OFF, Vout Low

Advantages:

- Near-zero static power in steady states
- High noise margins, good high-frequency performance

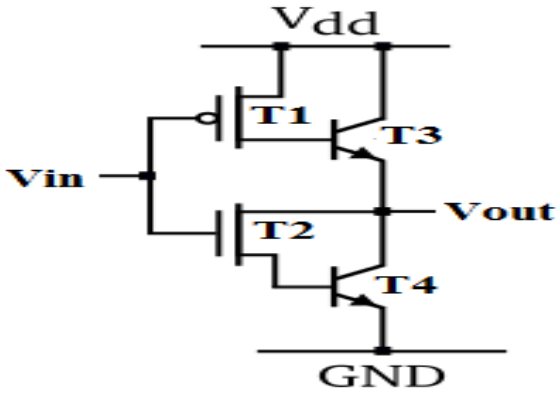
Applications:

Widely used in digital logic circuits for energy efficiency and high density.

Bi-CMOS Inverter Circuit

Configuration:

Combines CMOS transistors with BJTs in the output stage.



S. No	V_{in} (V_{GS})	T1	T2	T3	T4	V_{OUT}
1.	0 or Low	ON	OFF	ON	OFF	1
2.	1 or High	OFF	ON	OFF	ON	0

CMOS transistors handle input buffering and control, while BJTs offer fast switching and high current-driving capability.

Operation: CMOS controls the gate, and BJTs drive the output load.

Advantages: Faster switching and higher driving capacity, ideal for high-speed, high-frequency systems needing both digital and analog functionality.

UNIT- 4: Transistor Biasing and Thermal Stabilization

S. No	Topic Name
1.	Need for biasing,
2.	Operating point,
3.	Load line analysis,
4.	BJT biasing- methods, Fixed bias,Collector to base bias,Self bias
5.	Stabilization against variations in V_{BE}, Ic, and β,
6.	Stability factors, (S, S' , S''),
7.	Bias compensation,
8.	Thermal runaway, Thermal stability
9.	Introduction to Two-Port Network, Transistor Hybrid Model
10.	Determination of h-Parameters
11.	Conversion of h-Parameters
12.	Generalized Analysis of Transistor Amplifier using h-Parameters

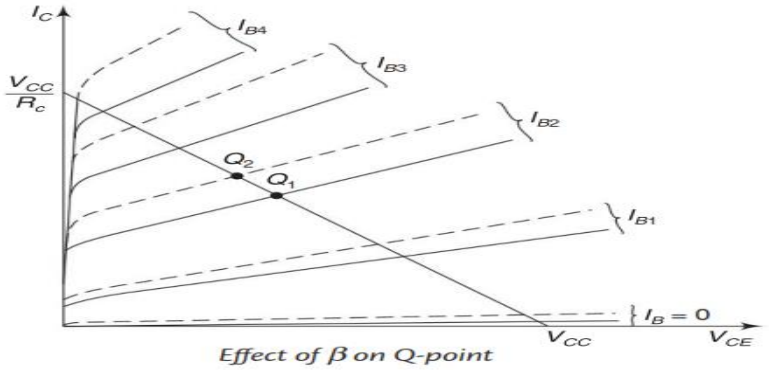
CLASS-29

NEED FOR BIASING:

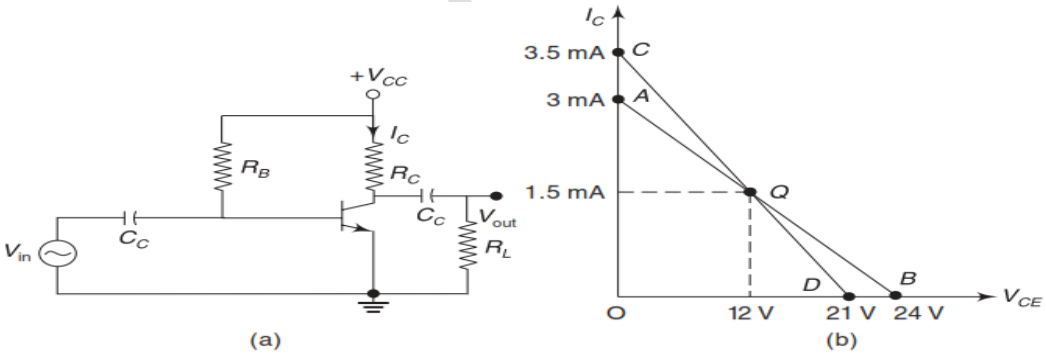
To produce distortion-free output, supply voltages and resistances must be chosen to set the quiescent values (VCEQ and ICQ), ensuring the transistor operates in the active region. This process, called biasing, establishes the operating point (Q-point) of the transistor, with circuits designed to achieve the desired Q-point.

The collector current for a common-emitter amplifier is expressed by

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (1 + \beta) I_{CO}$$



Effect of β on Q-point



(a) Biasing circuit (b) CE output characteristics and load line

Stability Factor (S) The extent to which the collector current I_C is stabilized with varying I_{CO} is measured by a stability factor S. It is defined as the rate of change of collector current I_C with respect to the collector-base leakage current I_{CO}, keeping both the current I_B and the current gain β constant.

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}, \beta \text{ and } I_B \text{ constant}$$

The collector current for a CE amplifier is given by

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

Differentiating Eq. (5.2) with respect to I_C, we get

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

Therefore, $$\left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta + 1)}{S}$$

$$S = \frac{1 + \beta}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

From this equation, it is clear that this factor S should be as small as possible to have better thermal stability.

Stability Factors S′ and S″ The stability factor S' is defined as the rate of change of I_C with V_{BE}, keeping I_{CO} and β constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}$$

The stability factor S'' is defined as the rate of change of I_C with respect to β, keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta}$$

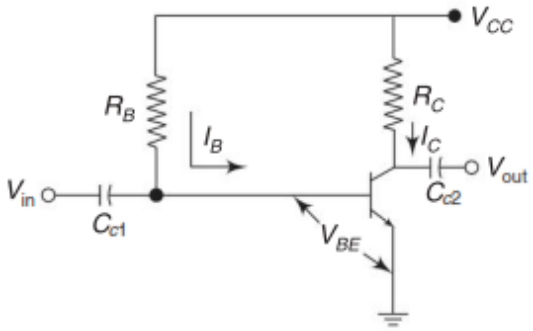
CLASS-30

BJT biasing- Methods:

Fixed Bias or Base Resistor Method :

A common-emitter amplifier using a fixed-bias circuit is shown in Following Figure

The dc analysis of the circuit yields the following equation.



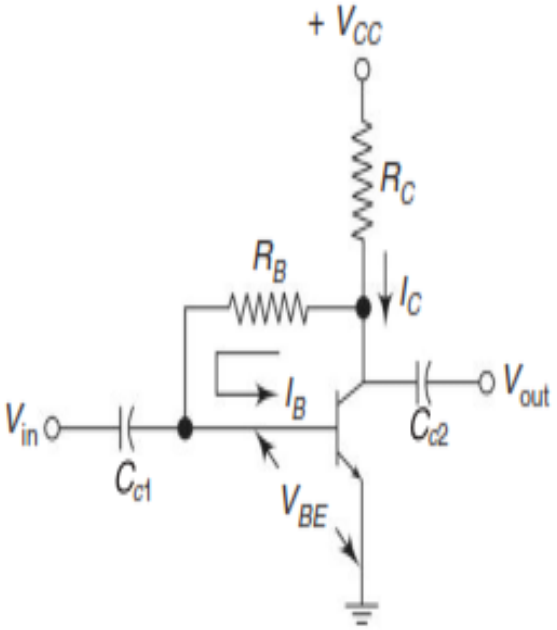
$$V_{CC} = I_B R_B + V_{BE}$$

Therefore, $$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Since this equation is independent of the current I_C, $dI_B/dI_C = 0$ and the stability factor given in Eq. (5.3) reduces to

$$S = 1 + \beta$$

Collector-to-Base Bias or Collector-Feedback Bias:



$$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE}$$

i.e., $$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B}$$

Therefore, $$\frac{dI_B}{dI_C} = \frac{-R_C}{R_C + R_B}$$

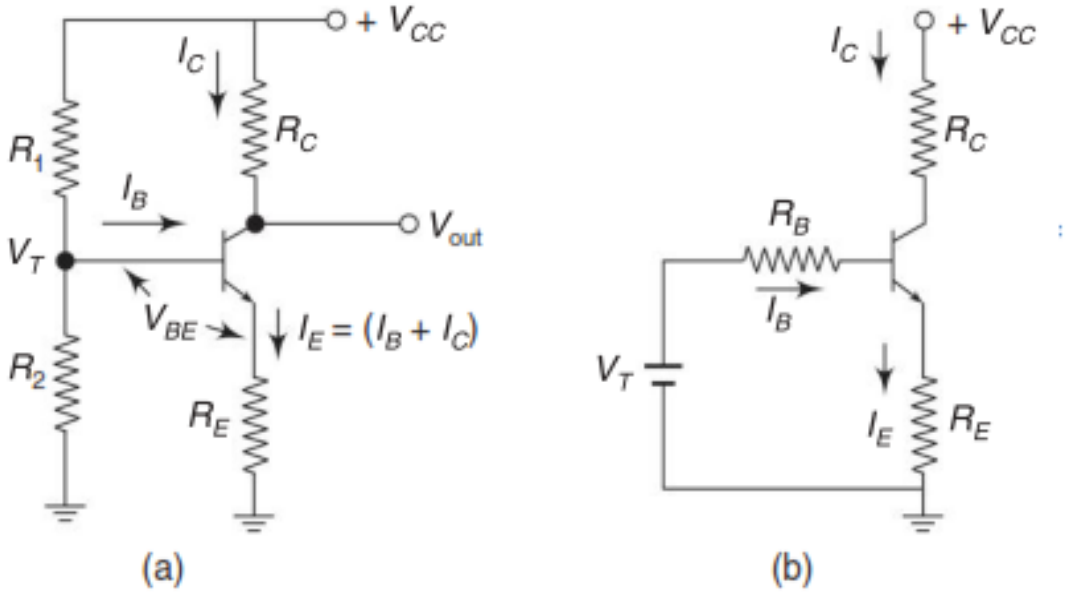
Substituting Eq. (5.17) into Eq. (5.3), we get

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C + R_B}\right)}$$

CLASS-31

Voltage-Divider Bias, Self-Bias, or Emitter Bias:

The self-biasing configuration, also known as emitter bias, uses a potential divider circuit for low collector resistance. The voltage drop across the emitter resistor RE reverse biases the emitter junction. To keep the transistor in the active region, the base-emitter junction is forward biased, with the required base bias supplied through the R1 and R2 potential divider network.



(a) Self-bias circuit (b) Thevenin's equivalent circuit

CLASS-32

Stabilization Factors - Stability factors, (S, S' , S'')

To Determine Stability Factor (S)

Applying Thevenin's theorem to the circuit of above figure, for finding the base current, we have

$$V_T = \frac{R_2 V_{CC}}{R_1 + R_2} \quad \text{and} \quad R_B = \frac{R_1 R_2}{R_1 + R_2}$$

The loop equation around the base circuit can be written as

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating this equation with respect to I_C, we get

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_E + R_B}$$

Substituting this equation in Eq. (5.3), we get

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_B}\right)}$$

Therefore,

$$S = (1+\beta)\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}}$$

To Determine the Stability Factor S$^{|}$

$$S' = \frac{dI_C}{dV_{BE}} = \frac{-\beta}{R_B + (1+\beta)R_E}$$

To Determine the Stability Factor S$^{||}$:

$$S'' = \frac{dI_C}{d\beta} = \frac{I_C}{\beta\left[1+\beta\left(\frac{R_E}{R_E + R_B}\right)\right]} = \frac{SI_C}{\beta(1+\beta)}$$

CLASS-33

Stabilization against variations in V_{BE}, I_C, and β

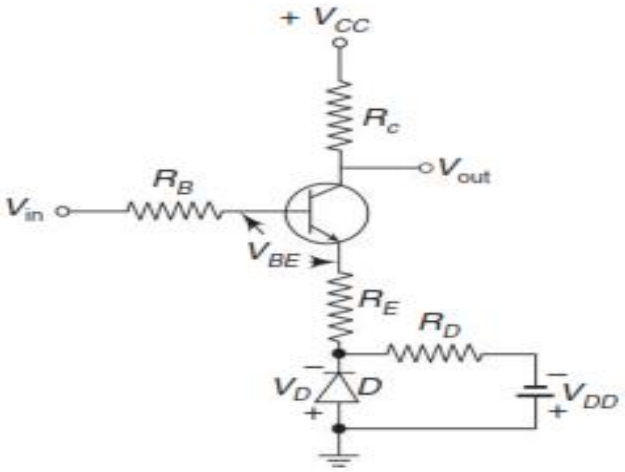
Compensation against Variation in V_{BE}, l_C and β:

Diode Compensation in Emitter Circuit:

Variation in V_{BE}

Diode Circuit is connected Emitter for achieving the desired Q-Point

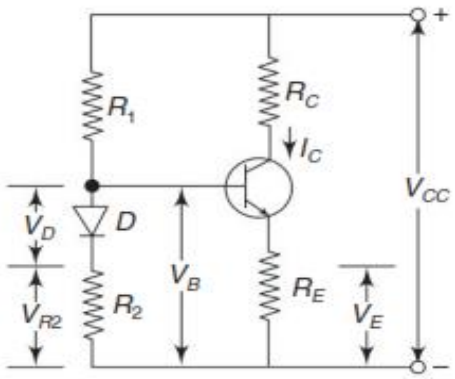
The various biasing circuits considered in the previous sections used some types of negative feedback to stabilize the operation point. Also, diodes, thermistors, and sensistors can be used to compensate for variations in current.



Stabilization by voltage-divider bias compensation

Variation in β :

Shows the diode compensation technique used in voltage-divider bias. Here, the diode is connected in series with the resistance R and it is in forward-biased condition. Therefore,



Diode compensation in voltage-divider bias circuit

$$I_E = \frac{V_E}{R_E} = \frac{V_B - V_{BE}}{R_E}$$

and $$I_C \approx I_E$$

When V_{BE} changes with temperature, I_C also changes. To cancel the change in I_C, a diode is used at the base terminal to compensate the change in V_{BE} as shown in Fig. The voltage at the base, V_B, becomes

$$V_B = V_{R2} + V_D$$

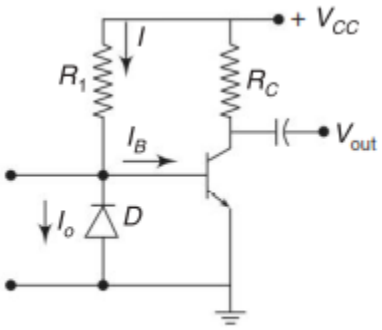
Substituting in the above equation for I_C, we get

$$I_C \approx \frac{V_{R2} + V_D - V_{BE}}{R_E}$$

CLASS-34

Variation in I_{CO}

Diode compensation in a transistor amplifier uses a diode (D) across the base-emitter junction to counter changes in collector saturation current ICO. The diode, made of the same material as the transistor, is reverse biased by VBE, allowing the diode's reverse saturation current I0 to flow. Thus, the base current IB = I - I0.



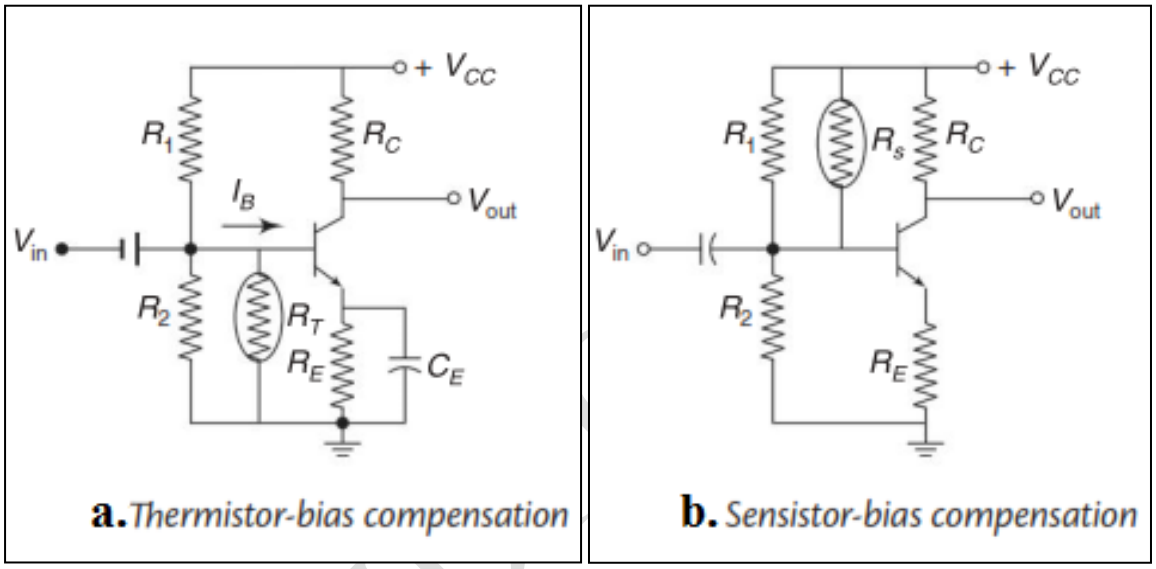
Diode-bias compensation

CLASS-35

Thermistor and SensistorCompensations :

Thermistor Compensation: A thermistor (RT) with a negative temperature coefficient is connected in parallel with R2. As temperature rises, RT's resistance decreases, lowering VBE, and reducing IB and IC. Bias stabilization is provided by RE and CE.

Sensistor Compensation: A sensistor (RS) with a positive temperature coefficient is connected across R1 (or RE). As temperature increases, RS's resistance rises, reducing the equivalent resistance of the parallel combination of R1 and RS.



CLASS-36

THERMAL RUNAWAY:

Thermal runaway is a condition where an increase in temperature causes a rise in current, which further increases the temperature, creating a dangerous cycle. In electronic components like transistors, if the temperature gets too high, the current through the component increases, which heats it up even more, potentially leading to failure if not controlled. It's like a vicious cycle where heat causes more heat, which can damage the component.

THERMAL STABILITY:

Thermal stability refers to a component's ability to maintain its performance without being affected by temperature changes. In electronics, it means that a device (like a transistor or circuit) should work consistently even when the temperature increases or decreases.

Introduction to Two-Port Network :

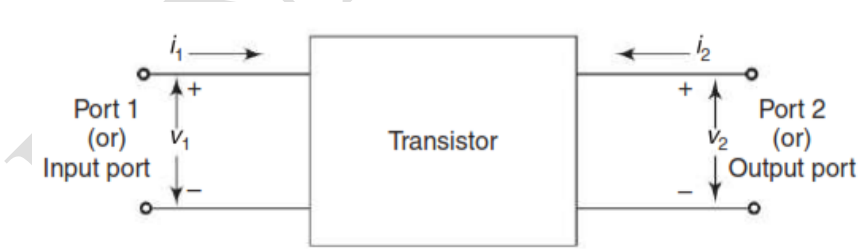
- **Input Port:** Terminals where input voltage (V_1) and input current (I_1) are applied.
- **Output Port:** Terminals where output voltage (V_2) and output current (I_2) are measured.

Mathematical Representation:

For a two-port network, the relations can be expressed in terms of hybrid (h)-parameters:

$$V_1 = h_{11}I_1 + h_{12}V_2$$

$$I_2 = h_{21}I_1 + h_{22}V_2$$



Two-port network

S.NO	h Parameter	Common Base Configuration	Common Emitter Configuration	Common Collector Configuration
1	h_{11}	h_{ib}	h_{ie}	h_{ic}
2	h_{12}	h_{rb}	h_{re}	h_{rc}
3	h_{21}	h_{fb}	h_{fe}	h_{fc}
4	h_{22}	h_{ob}	h_{oe}	h_{oc}

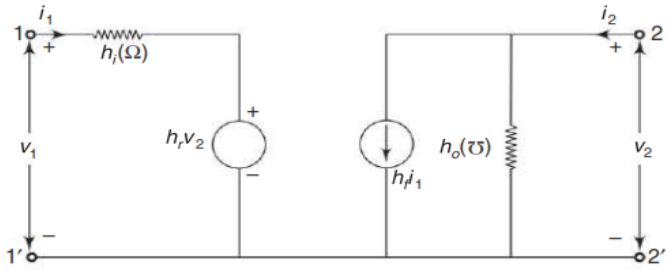
CLASS-37

Transistor Hybrid Model:

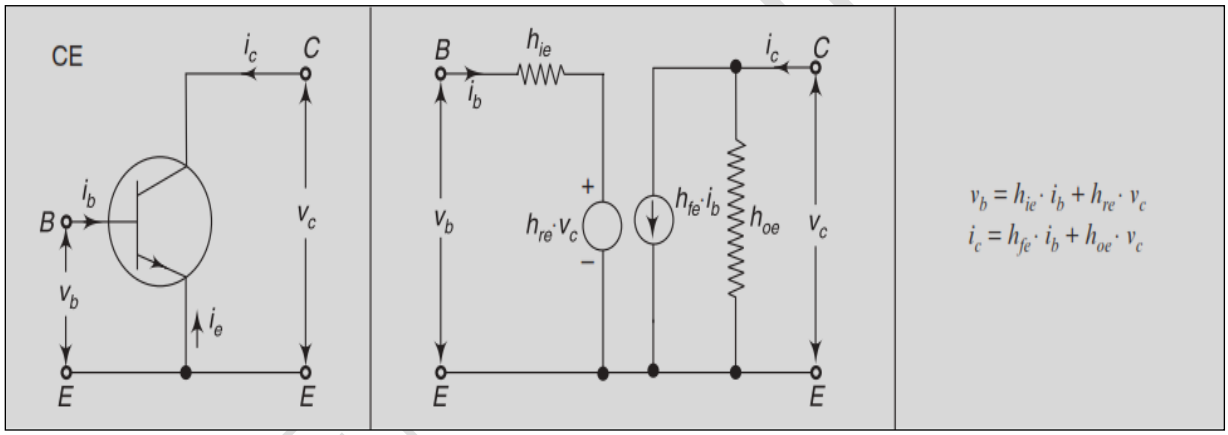
Based on the definition of hybrid parameters, the mathematical model for two-port networks known as *h*-parameter model can be developed. Equations and can be written as

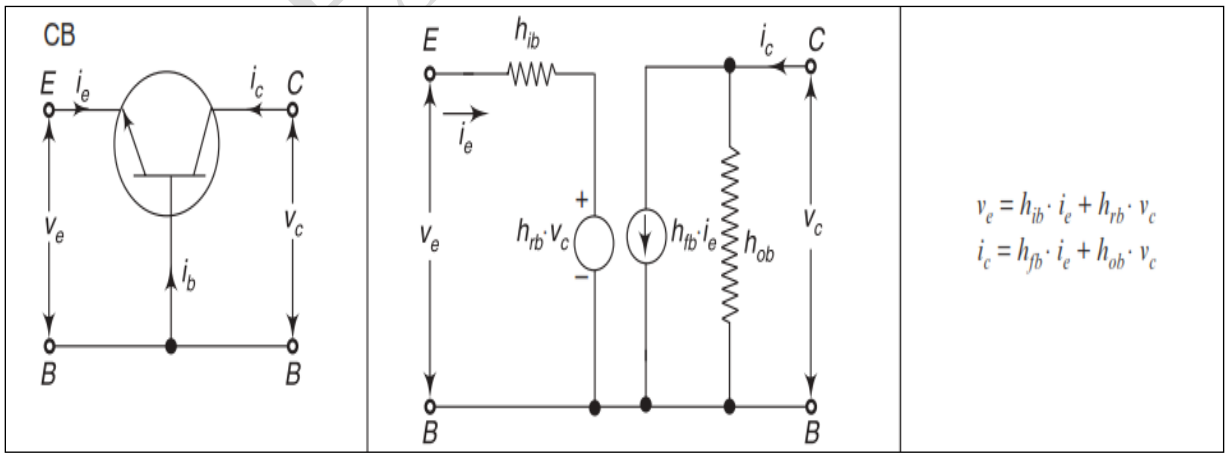
$$v_1 = h_i i_1 + h_r v_2$$
$$i_2 = h_f i_1 + h_o v_2$$

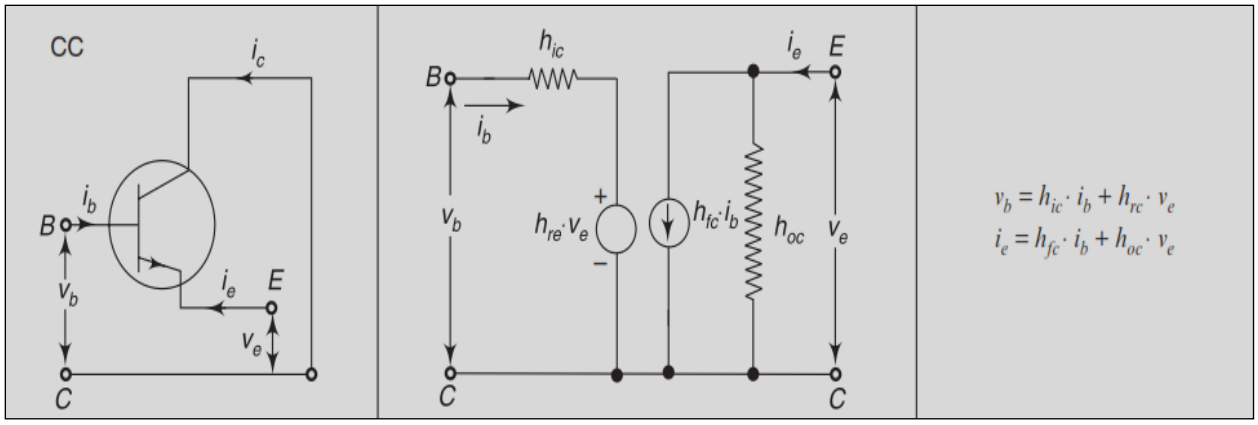
The proposed model shown in Fig. 6.2 should satisfy these two equations and it can be readily verified by writing Kirchhoff's voltage law equation in the input loop and Kirchhoff's current law equation for the output node. It is to be noted that the input circuit has a dependent voltage generator and the output circuit contains a dependent current generator.



Hybrid model for a two-port network







Determination of h-Parameters:

The four hybrid parameters h_{11}, h_{12}, h_{21}, and h_{22} are defined as follows:

$$h_{11} = \left[\frac{v_1}{i_1}\right] \text{ with } v_2 = 0$$

= input impedance with output port short-circuited

$$h_{22} = \left[\frac{i_2}{v_2}\right] \text{ with } i_1 = 0$$

= output admittance with input port open-circuited

$$h_{12} = \left[\frac{v_1}{v_2}\right] \text{ with } i_1 = 0$$

= reverse voltage gain with input port open-circuited

$$h_{21} = \left[\frac{i_2}{i_1}\right] \text{ with } v_2 = 0$$

= forward current gain with output port short-circuited.

$$\Delta v_b = \left(\frac{\partial f_1}{\partial i_b}\right)_{V_c} \Delta i_b + \left(\frac{\partial f_1}{\partial v_c}\right)_{I_b} \Delta v_c$$

$$\Delta i_c = \left(\frac{\partial f_2}{\partial i_b}\right)_{V_c} \Delta i_b + \left(\frac{\partial f_2}{\partial v_c}\right)_{I_b} \Delta v_c$$

$$h_{fe} = \frac{\delta i_C}{\delta i_B} = \left.\frac{\Delta i_C}{\Delta i_B}\right|_{V_C} = \frac{i_{C_2} - i_{C_1}}{i_{B_2} - i_{B_1}}$$

$$h_{oe} = \frac{\delta i_C}{\delta v_C} = \left.\frac{\Delta i_C}{\Delta v_C}\right|_{I_B}$$

$$h_{re} = \frac{\delta v_B}{\delta v_C} = \left.\frac{\Delta v_B}{\Delta v_C}\right|_{I_B} = \frac{v_{B_2} - v_{B_1}}{v_{C_2} - v_{C_1}}$$

$$h_{ie} = \frac{\delta v_B}{\delta i_B} = \left.\frac{\Delta v_B}{\Delta i_B}\right|_{V_C}$$

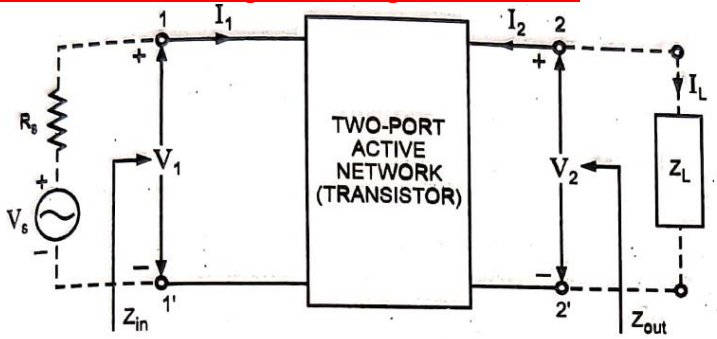
Conversion of h-Parameters:

CC	CB
$h_{ic} = h_{ie}$	$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$
$h_{rc} = 1$	$h_{rb} = \frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}$
$h_{fc} = -(1 + h_{fe})$	$h_{fb} = \frac{-h_{fe}}{1 + h_{fe}}$
$h_{oc} = h_{oe}$	$h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$

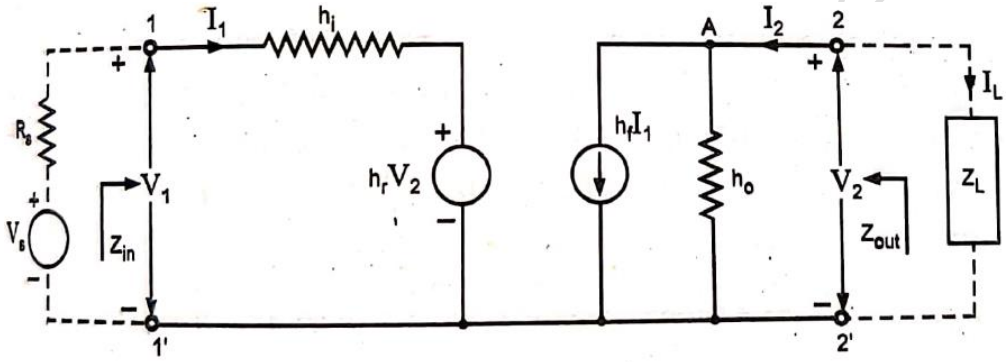
Configuration / Parameter	Common Emitter, CE	Common Base, CB	Common Collector, CC
h_{ie}	1.1 kΩ	$\frac{h_{ib}}{1 + h_{fb}}$	h_{ic}*
h_{re}	2.5×10^{-4}	$\frac{h_{ib} h_{ob}}{1 + h_{fb}} - h_{rb}$	$1 - h_{rc}$*
h_{fe}	50	$-\frac{h_{fb}}{1 + h_{fb}}$	$-(1 + h_{fc})$*
h_{oe}	25 μS (μA/V)	$\frac{h_{ob}}{1 + h_{fb}}$	h_{oc}*
h_{ib}	$\frac{h_{ie}}{1 + h_{fe}}$	21.6 Ω	$-h_{ic}/h_{fc}$
h_{rb}	$\frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}$	$2.9. \times 10^{-4}$	$h_{rc} - \frac{h_{ic} h_{oc}}{h_{fc}} - 1$
h_{fb}	$\frac{-h_{fe}}{1 + h_{fe}}$	−0.98	$-\frac{1 + h_{fc}}{h_{fc}}$
h_{ob}	$\frac{h_{oe}}{1 + h_{fe}}$	0.49 μS (μA/V)	$\frac{-h_{oc}}{h_{fc}}$
h_{ic}	h_{ie}*	$\frac{h_{ib}}{1 + h_{fb}}$	1.1 kΩ
h_{rc}	$1 - h_{re} \simeq 1$*	1	1
h_{fc}	$-(1 + h_{fe})$*	$\frac{-1}{1 + h_{fb}}$	−51
h_{oc}	h_{oe}*	$\frac{h_{ob}}{1 + h_{fb}}$	25 μS (μA/V)

CLASS-38

Generalized Analysis of Transistor Amplifier using h-Parameters



Basic Amplifier Circuit



Small Signal Hybrid Model of Transistor Amplifier

Current Gain:

The ration of output current to input current

Consider hybrid model equations

$v_1 = h_{11}i_1 + h_{12}v_2$--- (1)

$i_2 = h_{21}i_1 + h_{22}v_2$ --- (2)

$v_1 = h_{ie}i_1 + h_{re}v_2$--- (3)

$i_2 = h_{fe}i_1 + h_{oe}v_2$--- (4)

$A_I = \frac{i_L}{i_1}$

$A_I = \frac{-i_2}{i_1}$

$V_2 = i_L R_L$

$V_2 = -i_2 R_L$

Consider equation -4

$i_2 = h_{fe}i_1 + h_{oe}v_2$

$i_2 = h_{fe}i_1 + h_{oe}(-i_2R_L)$

$i_2 + h_{oe}i_2R_L = h_{fe}i_1$

$i_2(1+ h_{oe}R_L) = h_{fe}i_1$

$\frac{i_2}{i_1} = \frac{h_{fe}}{1+h_{oe}R_L}$

$A_I = -\frac{h_{fe}}{1+h_{oe}R_L}$

Input Impedance:

$Z_I = \frac{V_1}{i_1}$

Consider equation -3

$v_1 = h_{ie}i_1 + h_{re}v_2$

$v_1 = h_{ie}i_1 + h_{re}(-i_2R_L)$

divide i_1

$\frac{V_1}{i_1} = [h_{ie}i_1 + h_{re}(-i_2R_L)] / i_1$

$Z_I = h_{ie} + h_{re}\left(-\frac{i_2}{i_1}\right)R_L$

$$Z_I = h_{ie} - \frac{h_{re}h_{fe}}{1 + h_{oe}R_L}R_L$$

$$Z_I = h_{ie} - \frac{h_{re}h_{fe}}{\frac{1}{R_L} + h_{oe}}$$

Output Impedance:

$Z_{out} = \frac{V_2}{I_2}$

Consider equation - 4

$i_2 = h_{fe}i_1 + h_{oe}v_2$

$Z_{out} = v_2/(h_{fe}i_1 + h_{oe}v_2)$ -- (a)

from input port circuit shown in above

write loop equation and V_s as Zero

$R_S\, i_1 + h_{ie} i_1 + h_{re} v_2 = 0$

$(R_S + h_{ie}) i_1 = -h_{re} v_2$

$$i_1 = -\frac{h_{re} v_2}{h_{ie} + R_s}$$

this i_1 substitute in equation (a)

$$Z_O = \frac{v_2}{h_f\left(-\frac{h_{re} v_2}{h_{ie}+R_S}\right) + h_o v_2}$$

$$Z_O = \frac{R_s + h_{ie}}{h_{oe} R_S + (h_i h_o - h_f h_r)}$$

$$\Delta h = (h_i h_o - h_f h_r)$$

$$Z_O = \frac{R_s + h_{ie}}{h_{oe} R_S + \Delta h}$$

Output Admittance:

$Y_{out} = \frac{i_2}{v_2}$

Consider equation - 4

$i_2 = h_{fe} i_1 + h_{oe} v_2$

$Y_{out} = (h_{fe} i_1 + h_{oe} v_2)/v_2$

$$Y_{out} = h_{fe} \frac{i_1}{v_2} + h_{oe}$$

from input port circuit shown in above

write loop equation and V_s as Zero

$R_S\, i_1 + h_{ie} i_1 + h_{re} v_2 = 0$

$$\frac{i_1}{v_2} = -\frac{h_{re}}{h_{ie} + R_s}$$

$$Y_{out} = h_{oe} + h_{fe} \frac{i_1}{v_2}$$

$$Y_{out} = h_{oe} - h_{fe} \frac{h_{fe} h_{re}}{h_{ie}+R_S}$$

Another Method:

$$I_2 = h_f I_1 + h_o V_2$$

Dividing by V_2,

$$\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o$$

With $V_s = 0$, by KVL in the input circuit,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$I_1 (R_s + h_i) + h_r V_2 = 0$$

Hence, $$\frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i}$$

$$\frac{I_2}{V_2} = h_f\left(\frac{-h_r}{R_s + h_i}\right) + h_o$$

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s}$$

Voltage Gain:

$A_V = \frac{V_2}{V_1}$

$V_2 = -i_2 R_L$

$A_V = \frac{-I_2 R_L}{V_1}$

$A_I = \frac{-i_2}{i_1}$

$-i_2 = A_I i_1$

$A_V = \frac{A_I i_1 R_L}{V_1}$

$A_V = \frac{A_I R_L}{\frac{V_1}{i_1}}$

$A_V = \frac{A_I R_L}{Z_I}$

$A_I = -\frac{h_{fe}}{1 + h_{oe} R_L}$

$Z_I = h_{ie} - \frac{h_{re} h_{fe}}{\frac{1}{R_L} + h_{oe}}$

substitute A_I an Z_I in A_V

doing simple mathematics

$A_v = -\frac{h_{fe} R_L}{h_i + \Delta h R_L}$

$\Delta h = (h_i h_o - h_f h_r)$

Another Method(Simple)

$A_V = \frac{v_2}{V_1}$

$A_V = \frac{-I_2 R_L}{Z_I i_1}$

$A_V = A_I \frac{R_L}{Z_I}$

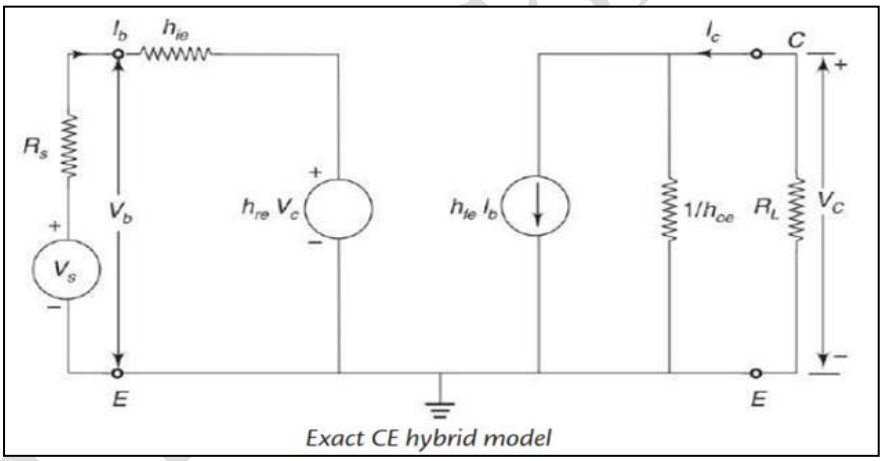
UNIT- 5: Small Signal Transistor Amplifier Circuits

S. No	Topic Name
1.	Low Frequency BJT & FET Amplifier Circuits: Analysis of CB, CE and CC Amplifiers using h-Parameter Model
2.	Comparison of BJT Transistor Amplifiers
3.	FET Small Signal Model,
4.	Comparison of FET Amplifiers.
5.	High Frequency BJT & FET Amplifier Circuits: High Frequency Transistor Models
6.	Hybrid-π models
7.	CE Current Gain
8.	Basic High-Frequency Analysis of FET Amplifier Circuits (Common Source and Common Drain)

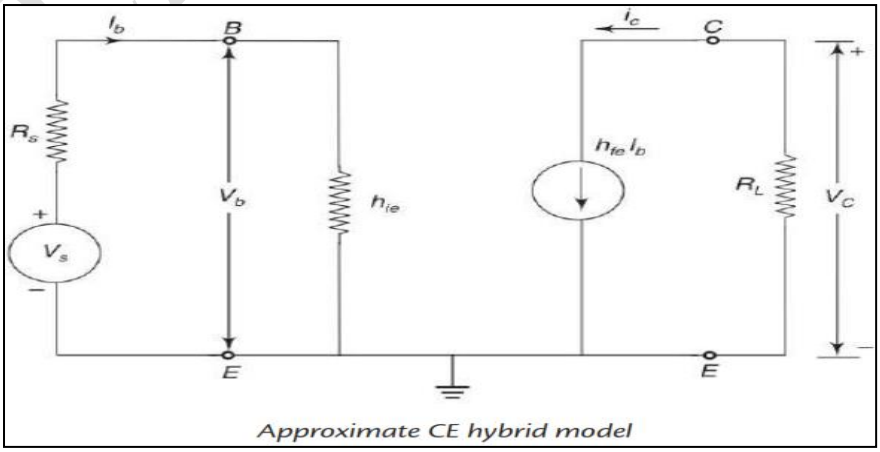
CLASS-39

Low Frequency BJT & FET Amplifier Circuits:

Analysis of CB, CE and CC Amplifiers using h-Parameter Model :



Exact CE hybrid model

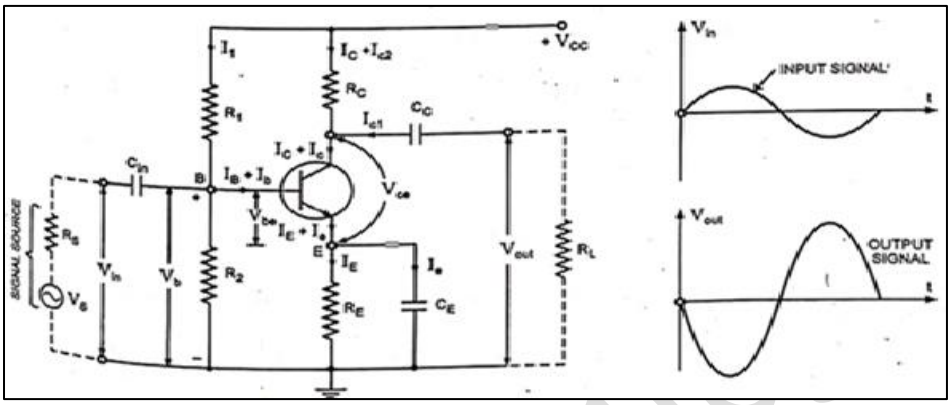


Approximate CE hybrid model

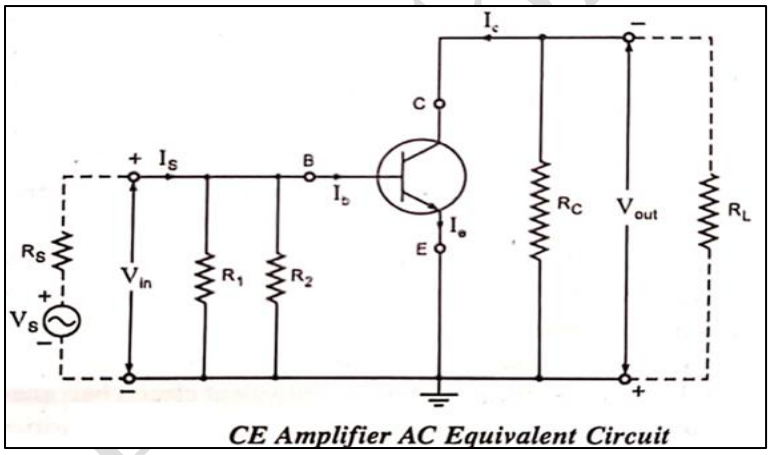
Analysis of CE Transistor Amplifier Using h Parameters:

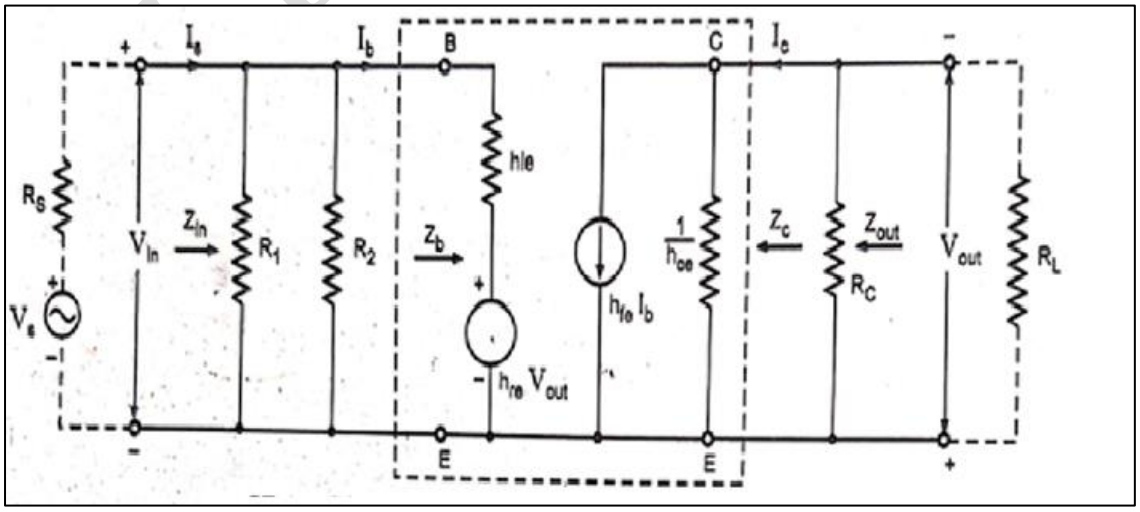
In AC analysis, the DC supply is grounded, and capacitors act as short circuits.

A common-emitter amplifier with self-biasing uses an NPN transistor. The input signal is applied to the base-emitter circuit, and the output is taken from the collector-emitter circuit. VCC forward biases the emitter-base junction and reverse biases the collector-emitter junction. When the input AC signal increases positively, VBE rises, increasing base current.



Common Emitter Transistor Amplifier Circuit with self biasing





CE - AMPLIFIER h parameter Equivalent circuit

CLASS-40

1. Input Impedance.

When looking into the base emitter terminals of the transistor, h_{ie}s seen to be in series with$h_{re}V_{out}$. For a CE circuit, h_{re} is normally a very small quantity, so $h_{re}v_{out}$fed back from the output to the input circuit is negligibly small as compared to the voltage drop across h_{ie}Thus,

$$Z_{in}(base) or z_b = h_{ie}$$

With an unbypassed emitter resistance $R_E$in the circuit, the computation of $z_b$becomes a little more complicated.

From the circuit shown in figure$h_{re}V_{out}$ being neglected, we have

$$\begin{aligned} V_{in} &= h_{ie}I_b + I_eR_E = h_{ie}I_b + R_E(I_b + I_c) \because I_e = I_b + I_c \\ &= I_b h_{ie} + I_b R_E + h_{fe} I_b R_E \because I_c = h_{fe} I_b \\ &= I_b[h_{ie} + R_E(1+h_{fe})] \end{aligned}$$

and input impedance to the transistor base,

$$Z_b = \frac{V_{ib}}{I_b} = h_{ie} + R_E(1 + h_{fe})$$

The actual circuit input impedance is$R_1||R_2||Z_b$so we have

$$Z_{in} or Z_{in}(stage) = R_1||R_2||Z_b$$

2. Output Impedance. Since the output voltage variations have little effect upon the input of a CE circuit, only the output of the circuit need be considered in determining the output impedance. Looking back into the collector and emitter terminals of the...

$$V_{in} = h_{ie}I_b + I_eR_E = h_{ie}I_B + R_E(I_b + I_C)$$

The actual circuit output impedance is $Z_c$in parallel

$$Z_{out} = \frac{1}{h_{oe}} ||R_c$$

Since$\frac{1}{h_{oe}}$is typically 1 MΩ or so, and$\boldsymbol{R_c}$is usually very much less than 1 MΩ, the circuit output impedance Z_{out} is approximately equal to R_c

3. Voltage Gain.

It is given as the ratio of output voltage to the input voltage (A_V)

i.e

$$\begin{aligned} A_V = \frac{V_{out}}{V_{in}} &= \frac{-I_c Z_{ac}}{I_b Z_{in}} = \frac{-I_c(R_c||R_L)}{I_b h_{ie}} \\ &= \frac{-\boldsymbol{h_{fe} I_b (R_c||R_L)}}{\boldsymbol{I_b h_{ie}}} \\ &= \frac{-\boldsymbol{h_{fe}}}{\boldsymbol{h_{ie}}} (R_c||R_L) \end{aligned}$$

The minus sign indicates that output voltage $\boldsymbol{V_{out}}$is 180° out of phase with input voltage $\boldsymbol{V_{in}}$

With an un bypassed emitter resistance $R_E$in the circuit

Ignoring $\boldsymbol{h_{re}V_{out}}$we have from the input loop of the circuit

$$V_{in} = I_b h_{ic} + I_e R_E = I_b h_{ie} + R_E(I_b + I_c)$$
$$= I_b h_{ie} + R_E I_b(1 + h_{fe})$$
$$= I_b[h_{ie} + R_E(1 + h_{fe})]$$

and voltage gain

$$\mathbf{A_V = \frac{V_{out}}{V_{in}} = \frac{-I_c(R_C \,||R_L)}{I_b[h_{ie}+R_E(1+h_{fe})]} = \frac{-h_{fe}(R_C||R_L)}{h_{ie}+R_E(1+h_{fe})}}$$
$$Usually R_E(1 + h_{fe}) \gg h_{ie}\,, therefore,$$
$$A_V \cong \frac{-R_C \,||R_L}{R_E}$$

***4.* Current Gain.** *It is given as the ratio of output current to the input current i.e.,*

$$A_V = \frac{I_L^*}{I_b} = \frac{-I_C}{I_b} = -h_{fe}$$

$I_b = \frac{I_S R_B}{R_B Z_b}$ and $I_C = h_{fe} I_b = \frac{h_{fe} I_S R_B}{R_B Z_b}$

Current gain without external load RLR_LRL in the circuit,

$$= \frac{-I_c}{I_s} = \frac{-h_{fe} R_B}{R_B Z_b}$$

Overall current gain with external load RLR_LRL in the circuit,

$-Ic = R_B Z_b - h_{fe} R_B$

Power Gain. $A_p = A_v A_i$

Analysis of CB Transistor Amplifier Using h Parameters:

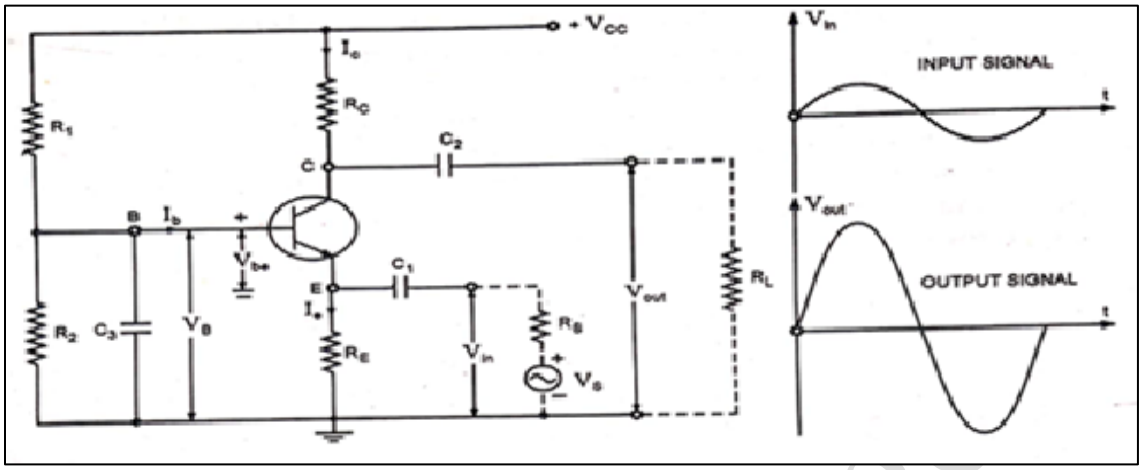
A practical common-base amplifier uses emitter current bias. The AC signal is applied to the emitter through coupling capacitor C1C_1, and the load resistor RLR_L is connected to the collector via C2C_2. Capacitor C3C_3 AC shorts the base to ground.

The emitter-base junction is forward biased, and the collector-base junction is reverse biased. With the base AC shorted to ground, the input voltage at the emitter appears across the base-emitter junction.

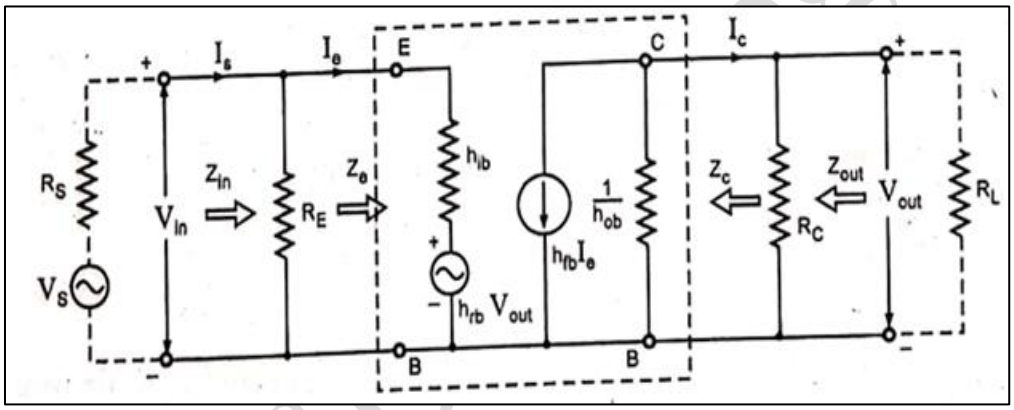
When the signal is applied, a positive half-cycle reduces VBEV_{BE} since VBV_B remains constant. This decreases base current IBI_B, leading to a reduction in collector current ICI_C and emitter current IEI_E, both approximately β\beta times.

CLASS-41

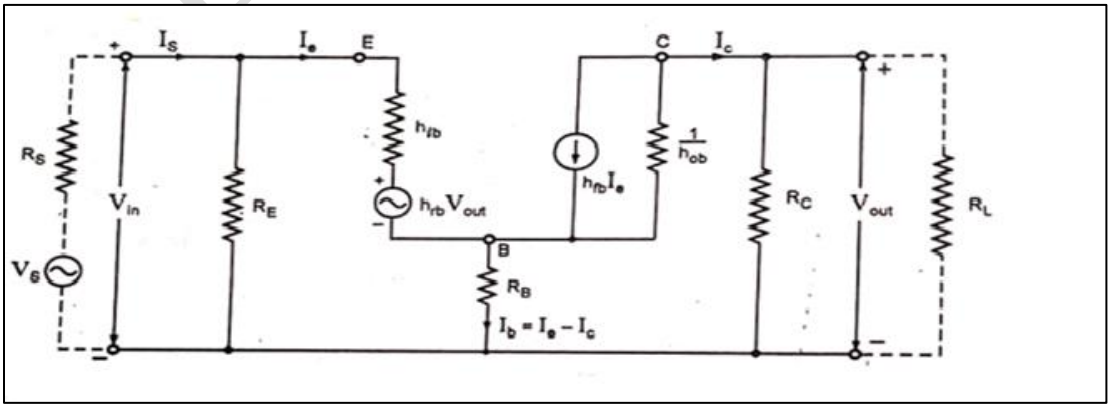
Common Base Transistor Amplifier Circuit With Emitter Current Bias



CB Amplifier h Parameter Equivalent Circuit



- AC Equivalent Circuit: DC supply is replaced by a short circuit; capacitors act as short circuits.
- Operation: V_{IN} is applied across the emitter-base, and VOUT is taken from the collector-base. The base is common to both, hence called a common-base or grounded-base circuit.
- h-Parameter Model: The transistor is replaced with its h-parameter equivalent.



CB Amplifier h Parameter Equivalent Circuit With Bypass Capacitor at Transistor Base Terminal

CLASS-42

1. Input Impedance. The input impedance to the transistor emitter is given as

$$Z_e \approx h_{ib}$$

From circuit given in Figure

$$V_{in} = h_{ib}I_e + I_b X R_B$$
$$= h_{ie}I_e + I_e R_B - I_C I_B \because I_b = I_e - I_c, I_c = -h_{fb}I_e$$
$$= I_e[h_{ib} + R_B(1 + h_{fb})]$$

and input impedance to the transistor emitter,

$$Z_e = \frac{V_{in}}{I_e} = h_{ib} + R_B(1 + h_{fb})$$

The actual circuit input impedance is parallel combination of $\boldsymbol{Z_e}$ *and* $\boldsymbol{R_E}$,so we have

$$Z_{in} = Z_e \,||R_E$$

2. Output Impedance: Since the output voltage variations have little effect upon the input of a CB circuit, only the output of the circuit need be considered in determining the output impedance. Looking back into the collector and base terminals of the transistor in Fig, a large resistance $\frac{1}{h_{oe}}$ is seen. Thus the device output impedance

$$Z_C \approx \frac{1}{h_{ob}}$$

$$Z_{out} = \frac{1}{h_{ob}} ||R_C$$

Since $\frac{1}{h_{ob}}$ is of the order of MΩ, and R_C is quite small as compared to$\frac{1}{h_{ob}}$, the circuit output impedance $Z_{out}$is approximately equal toR_C.

3. Voltage Gain:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{I_C Z_{ac}}{I_e Z_{in}}$$
$$\approx \frac{I_C\,(R_C||R_L)}{I_e h_{ib}} \approx \frac{-h_{fb}(R_C||R_L)}{h_{ib}}$$

Because of the negative value of $\boldsymbol{h_{fb}}$ the output voltage $\boldsymbol{V_{out}}$ and input voltage $\boldsymbol{V_{in}}$are in phase.

When the bypass capacitor c_3 at the base terminal is connected.

Output voltage,

$$V_{out} = I_C(R_c||R_L)$$

Input voltage,

$$V_{in} = I_e[h_{ib} + R_B(1 + h_{fb})]$$Refer to Eq,,,

So voltage gain,

$$A_V = \frac{V_{out}}{V_{in}} = \frac{-h_{fb}\,(R_C\,||R_L)}{h_{ib} + R_B(1 + h_{fb})}$$

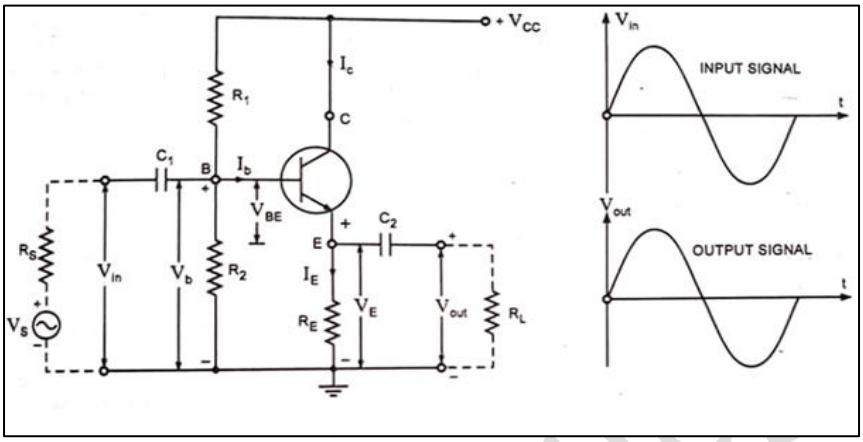
4. Current Gain:

$$A_i = \frac{I_C}{I_E} = -h_{fb}$$

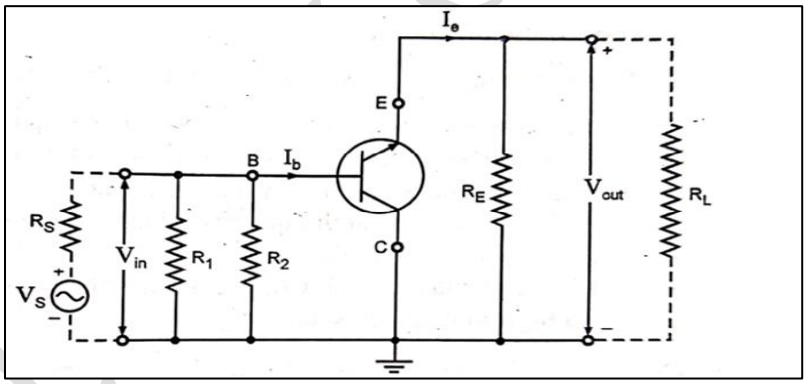
CLASS-43

Analysis of CC Transistor Amplifier Using h Parameters:

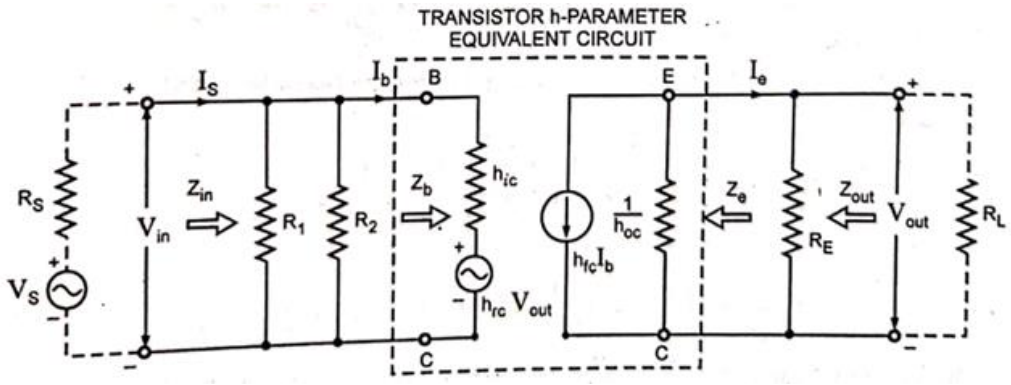
CommonCollector Transistor Amplifier Circuit With Emitter Current Biasing



Circuit Analysis: The common-collector AC equivalent circuit is formed by replacing the DC supply and capacitors with short circuits. The input is at the base-collector terminals, and the output is at the emitter-collector terminals. Since the collector is common to both, it is called a common-collector or grounded-collector circuit.



Common Collector AC Equivalent Circuit



CC Amplifier h Parameter Equivalent Circuit

CLASS-44

1. Input Impedance. The noteworthy point in CC amplifier is that h_{rc}=1 *i.e.*, all of the V_{out} is fed back to the input. Thus

$$\text{Input voltage,} V_{in} = h_{ie}I_b + V_{out}$$
$$= h_{ie} I_b + I_e(R_E||R_L)$$
$$= h_{ic}I_b - h_{fc}I_b(R_E||R_{L)}$$
$$= I_b[h_{ic} - h_{fc}(R_E||R_L)$$

The input impedance to the transistor base,

$$Z_b = \frac{V_{in}}{I_b}$$
$$= h_{ic} - h_{fc}(R_E\,||R_L)$$
$$= Z_{in} = Z_b\,||R_1\,||R_2$$

2. Output Impedance:

In the common collector circuit, any variation in output voltage has a significant effect on the input circuit

$$Z_e = \frac{V_{out}}{I_e} \text{and} I_e = -h_{fc}I_b$$

With input signal voltage, $\boldsymbol{V_s}$=0, I_b is produced by $\boldsymbol{V_{out}}$.

$$I_b = \frac{V_{out}}{h_{ic} + (R_1||R_2||R_s)}$$

$$\text{and } I_e = -h_{fc}I_b = \frac{-h_{fc}V_{out}}{h_{ic}+(R_1||R_2||R_s)}$$

$$\text{so,} Z_e = \frac{V_{out}}{I_e} = \frac{-h_{ic}+(R_1||R_2||R_s)}{h_{fc}}$$

The above equation gives the output impedance of the device only. For the circuit output impedance,$\boldsymbol{R_E}$ is in parallel with $\boldsymbol{Z_e}$ so,

$$Z_{out} = Z_e\,||R_E$$

Since$\boldsymbol{R_E}$ is usually much larger than $\boldsymbol{Z_E}$

$$z_{out} = Z_e$$

3. Voltage Gain:

Output voltage,

$$\boldsymbol{V_{out} = I_e(R_E||R_L) = -h_{fe}I_b(R_E||R_L \because I_e = -h_{fe}I_b}$$

and input voltage

$$\boldsymbol{V_{in} = I_b[h_{ic} - h_{fc}(R_E\,||R_L)]}$$

So voltage gain,

$$\mathbf{A_v = \frac{V_{out}}{V_{in}} = \frac{-h_{fe}(R_E||R_L)}{h_{ic} - h_{fc}(R_E\,||R_L)}}$$
$$= \frac{-h_{fc}(R_E||R_L)/h_{ic}}{1-\frac{h_{fc}(R_E||R_L)}{h_{ic}}} \cong \mathbf{1}$$

4. Current Gain:

Current gain,

$$\mathbf{A_i} = \frac{\mathbf{I_e}}{\mathbf{I_b}} = -\mathbf{h_{fe}} \therefore I_e = -h_{fe} I_b$$

$$\mathbf{A_i} = \frac{-\mathbf{h_{fe}} \mathbf{R_B} \mathbf{R_E}}{(\mathbf{R_B} + \mathbf{Z_b})(\mathbf{R_L} + \mathbf{R_E})}$$

Amplifier Type	Characteristics	Applications
Common-Base (CB)	- Current gain < 1, decreases with RL	- Matching low-impedance sources
	- High voltage gain	- Non-inverting amplifier with voltage gain > 1
	- Lowest input resistance	- Driving high-impedance loads
	- Highest output resistance	- Constant current source
Common-Collector (CC) (Emitter Follower)	- High current gain for RL < 10kΩ	- Used as a buffer between high-impedance sources and low-impedance loads
	- Voltage gain < 1	
	- Highest input resistance	
	- Lowest output resistance	
Common-Emitter (CE)	- High current gain for RL < 10kΩ	- Provides both voltage and current gain
	- High voltage gain	- Most widely used for amplification
	- Medium input resistance	
	- Moderately high output resistance	

CLASS-45

Generalized Analysis of FET Small Signal Model:

FET Amplifier Configurations & Characteristics

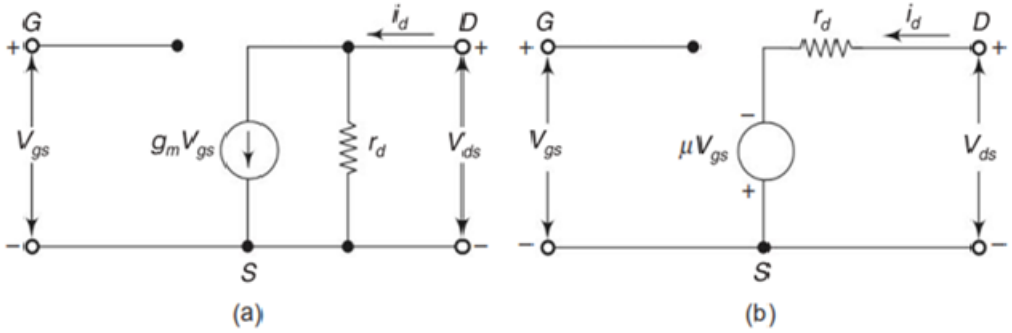
- Common-Source (CS): Good voltage amplification, most commonly used.
- Common-Drain (CD) (Source-Follower): High input impedance, near-unity voltage gain, used as a buffer.
- Common-Gate (CG): High-frequency amplifier.

Small-Signal Models:

- CS uses a current-source model with Thevenin's equivalent for voltage-source.
- Key parameters: μ (amplification factor), r_d (drain resistance), g_m (mutual conductance).

FET Amplifier Advantages:

- High input impedance, low power consumption, wide frequency range.
- Small size, low noise, ideal for small-signal amplification.
- JFETs, depletion MOSFETs, and enhancement MOSFETs have similar voltage gains; depletion MOSFETs offer higher input impedance.
- Minimal input current (microamperes) due to high input impedance, making current gain undefined.
- Output impedance similar to BJT circuits.



(a) Small-signal current-source model for FET in CS configuration
(b) Voltage-source model for FET in CS configuration

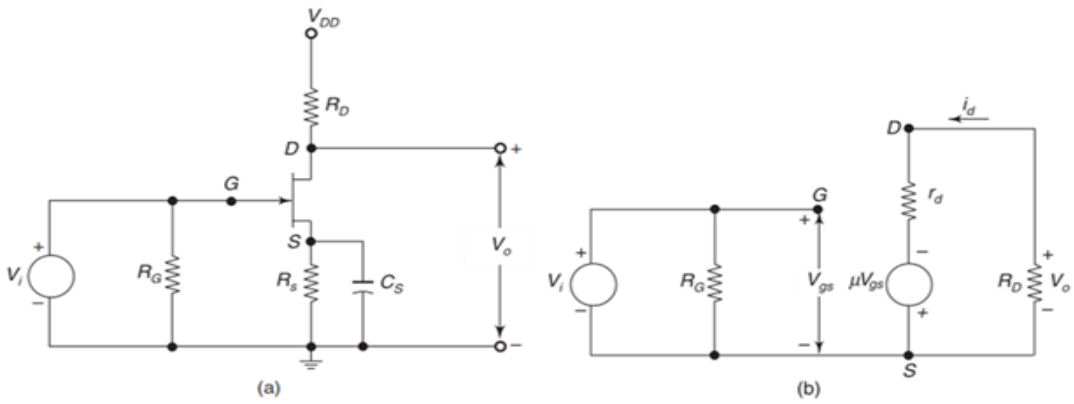
Voltage Gain:

Source resistor R_s is used to set the Q-point but is bypassed by C_S for mid-frequency operation.
From the small-signal equivalent circuit, the output voltage,

$$\boldsymbol{V_o = \frac{-R_D}{R_D + r_d}\mu V_{gs}}$$

where $V_{gs} = V_i$, the input voltage.
Hence, the voltage gain,

$$\boldsymbol{A_V = \frac{V_d}{V_i} = \frac{-\mu R_D}{R_D + r_d}}$$



(a) Common source amplifier (b) Small-signal equivalent circuit of CS amplifier

Input Impedance

From figure the input impedance is given by

$$\boldsymbol{Z_i = R_G}$$

For voltage divider bias as in **CE** amplifiers of **BJT**,

$$\boldsymbol{R_G = R_1 || R_2}$$

Output Impedance

Output impedance is the impedance measured at the output terminals with the input voltage $V_i = 0$.

From Fig., when $V_i = 0, V_{gs} = 0$ and hence,

$$\boldsymbol{\mu V_{gs} = 0}$$

Then the equivalent circuit for calculating output impedance is given in Fig.

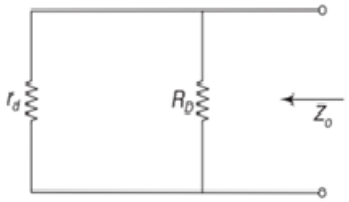
Output impedance

$$\boldsymbol{Z_o = r_d || R_D}$$

Normally, r_d will be far greater than R_D.

Hence,

$$\boldsymbol{Z_o = R_D}$$



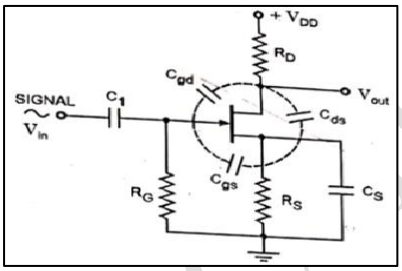
CLASS-46

Comparison of FET Amplifiers

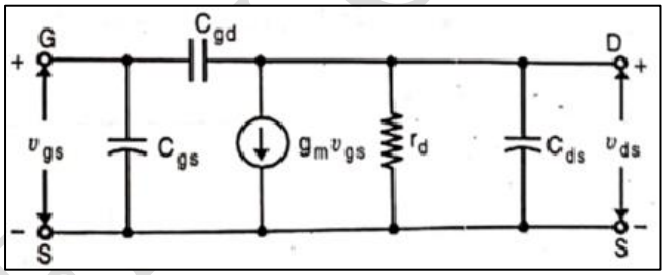
Circuit configuration	Z_i	Z_o	A_v	Phase shift
CS	$\approx R_G$	$\approx R_D$	$-Y_{fs}(R_D \| R_L)$	180°
CD	$\approx R_G$	$\approx 1/Y_{fs}$	≈ 1	0
CG	$\approx 1/Y_{fs}$	$\approx R_D$	$Y_{fs}(R_D \| R_L)$	0

High Frequency BJT & FET Amplifier Circuits: High Frequency Transistor Models:

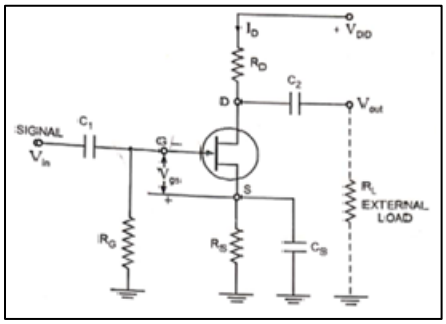
At low frequencies, inter-electrode capacitances have high reactance and are negligible in the equivalent circuit. At higher frequencies, device and stray wiring capacitances reduce amplifier gain as capacitive impedance decreases with frequency. These unintentional capacitances, shown with dashed lines in the circuit, result from device construction and wiring.



High Frequency Model of FET



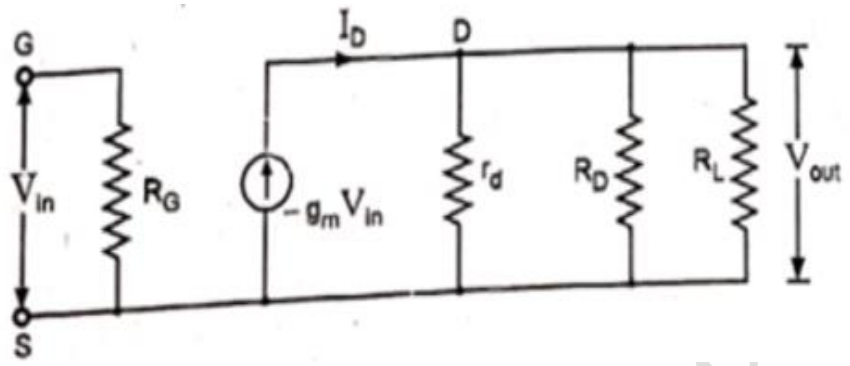
Common Source Amplifier Circuit:



- Capacitor Polarity: Negative terminal of polarized capacitors must be at a lower DC potential to avoid performance issues.
- Bypass Capacitor (CSC_S): Grounds the FET source, ensuring full input voltage across gate-source terminals, affecting ID.
- Phase Relationship:

- Positive Vin reduces Vgs, increasing ID, causing VDV to drop.
- Negative Vin increases Vgs, reducing ID, causing VDV to rise.
- Vout is 180° out of phase with Vin.

- AC Analysis: Replace capacitors with short circuits and set DC voltages to zero for the AC equivalent circuit.



Input Resistance: In an ideal JFET R_{gs} is infinite because I_G=0. However, in actual device R_{gs} is not infinite but extremely high (100 MΩ or so) in comparison to R_G. Thus, input resistance

$$R_{in} = R_G \,||R_{gs} \approx R_G$$

Output Resistance:

$$Z_d \approx r_d$$

Z_d is the device output impedance; the circuit output impedance is R_D in parallel with Z_d so

$$Z_{out} = R_D \,||Z_d = R_D \parallel r_d$$

Since usually $\boldsymbol{r_d \gg R_D}$, the circuit output impedance is taken to be R_D.

Voltage Gain:

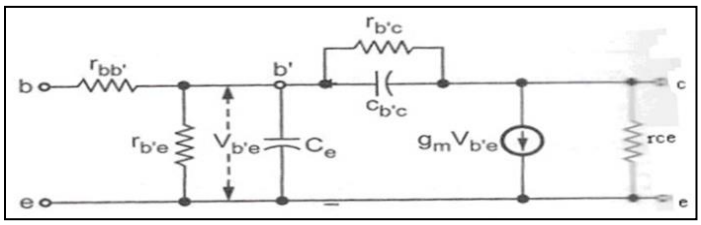
$$A_v = \frac{V_{out}}{V_{in}} = -g_m(r_d||R_D||R_L)$$

Usually $r_d \gg R_D||R_L$
So voltage gain,

$$A_v = -g_m(R_D||R_L)$$

The minus sign indicates that output voltage $\boldsymbol{v_{out}}$ is 180∘ out of phase with input voltage $\boldsymbol{v_{in}}$

Full - Hybrid - π Model



r_π is base emitter internal resistance (r_{be})
gm - transconductance
$r_\pi = \frac{V_{be}}{i_b}$

CLASS-47

Hybrid Pi Model

Input Resistance :R_I = R1|| R2|| r_π

$V_\pi = \frac{R_I V_S}{R_I + R_S}$

$V_O = -g_m v_\pi (r_o || R_L)$

$V_O = -g_m \frac{R_I V_S}{R_I + R_S} (r_o || R_L)$

$\frac{V_O}{V_S} = -g_m \frac{R_I}{R_I + R_S} (r_o || R_L)$

Voltage Gain

$A_V = -g_m \frac{R_I}{R_I + R_S} (r_o || R_L)$

Output Resistance:

$R_O = r_o || R_L$

CE Current Gain:

$\beta = r_\pi g_m$

CLASS-48

Basic High-Frequency Analysis of FET Amplifier Circuits (Common Source and Common Drain).

Common Drain Amplifier

In the common-drain (source follower) circuit, the output voltage is across the source resistor RSR_S, and the external load resistor RLR_L connects to the source through coupling capacitor C2C_2. The gate bias VGV_G is derived from VDDV_{DD} via a potential divider R1R_1 and R2R_2, with no resistor in the drain terminal and no source bypass capacitor. The input signal is applied through coupling capacitor C1C_1.

Operation:

- The gate voltage VGV_G remains constant, and when a signal is applied, it causes VgsV_{gs} to vary slightly.
- The source voltage VSV_S follows these changes in gate voltage, so the output voltage at the source is nearly the same as the input voltage.
- The circuit provides **unity gain**, and since the output follows the input signal, it is known as a **source follower**.
- The AC equivalent circuit shows current I=gmVgsI = g_m V_{gs}.

where $V_{gs}=V_{in}-V_{out}$

moreover $R_G = R_1 \,||R_2$

$$\text{or } V_{out} = g_m V_{gs}(r_d||R_S||R_L)$$

$$\text{and } V_{in} = v_{gs} + v_{out} = V_{gs} + V_{gs}g_m(r_d||R_S||R_L)$$

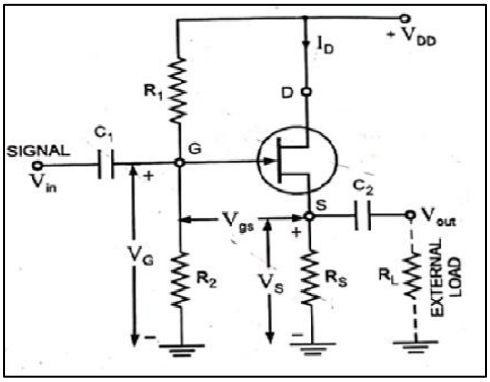
$$\therefore V_{gs} = V_{in} - V_{out}$$

$$\text{Voltage gain } A_v = \frac{V_{out}}{V_{in}} = \frac{g_m(r_d||R_S||R_L)}{1+g_m(r_d||R_S||R_L)}$$

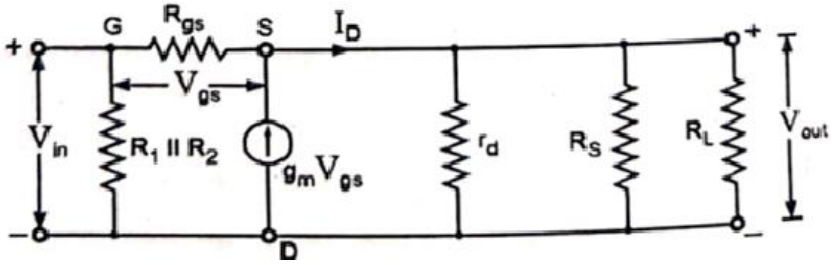
Normally $r_d \gg R_S \parallel R_L$

$$\therefore A_v = \frac{g_m(R_S||R_L)}{1 + g_m\,(R_S||R_L)}$$

If $\boldsymbol{g_m(R_S||R_L) \gg 1\ then\ A_V = 1}$



Common Drain Amplifier Circuit



AC Equivalent Circuit For Common Drain JFET Amplifier

So value of voltage gain becomes approximately equal to unity (slightly less than unity).

Input Impedance. The circuit input impedance is $\boldsymbol{R_G = R_1 \,||R_2}$

Output Impedance.

$$V_{gs} = V_{out} \times \frac{R_{gs}}{(R_S||R_G) + R_{gs}}$$

Normally

$$R_{gs} \gg R_S \;||R_G, \text{ so } V_{gs} = V_{out}$$

And $\boldsymbol{I_D = g_m V_{gs}}$

$$\text{Also } Z_S = \frac{v_{out}}{I_n} = \frac{v_{gs}}{g_m V_{gs}} = \frac{1}{g_m}$$

Actually ,$\boldsymbol{r_d}$is inparallel with $\frac{\mathbf{1}}{\boldsymbol{g_m}}$, *but* since$\boldsymbol{r_d} \gg \frac{\mathbf{1}}{\boldsymbol{g_m}}$,it is neglected $R_S$is the outut impedance of the device , the circuit output impedance 0

$$Z_{out} = R_S||\frac{1}{g_m}$$